MAINTENANCE

This section presents descriptive information about instrument calibration as well as preventive maintenance, corrective maintenance, and troubleshooting information. Circuit board removal procedures are included in the "Corrective Maintenance" subsection. An extensive diagnostics procedures table (Table 6-6) is in the "Diagnostics" subsection at the back of this section.

INSTRUMENT CALIBRATION

This oscilloscope uses automatic internal routines to calibrate itself as much as possible. These automatic routines minimize manufacturing and end-user costs associated with calibration and enhance the accuracy of the instrument during use.

Instead of the usual numerous manual potentiometer "tweaks" that require extensive servicing, the scope makes wide use of digital calibration techniques. The extensive digital-to-analog (DAC) subsystem of the scope and the built-in computer firmware are used to calculate and adjust more than 100 voltages that control gain, offset, and other parameters of circuit operation affecting accuracy. The automatic SELF CAL uses no external test equipment and takes less than 10 seconds to complete. The ease of use of SELF CAL allows it to be done at any time to ensure accurate measurements in the present testing environment.

Adjustments that remain are not automatic and require manual adjustment of components and/or user-supplied external standard test signals. The display system and CCD output amplifier gains require manual "tweaking," but the instrument provides the necessary test signals internally. The vertical attenuator and trigger amplifier calibrations require external signals, but the instrument performs the adjustments internally. Finally, the CCD clocks, input capacitance, bandwidth limit filters, and transient response adjustments which affect high frequency performance signals and internal both external require manual adjustments.

Calibration Levels

Instrument calibration occurs at several levels. These levels are the fully automatic SELF CAL, the semiautomatic EXTENDED CAL, the manual adjustments, and dynamic calibration.

Self Calibration

Almost all of the internal measurement systems are calibrated by performing the SELF CAL procedure. These automatic adjustments include the gain and offset settings for the vertical acquisition system and the internal trigger system. No adjustments are required for the time base or horizontal subsystems.

Maximum instrument accuracy can be assured by doing a SELF CAL just before making critical measurements. Continued accuracy is maintained by running SELF CAL whenever the operating temperature has changed more than five degrees Celsius since the last SELF CAL.

Extended Calibration

Semiautomatic calibration of the vertical attenuators (ATTEN) and external trigger amplifiers (TRIGGER) is supported by this level of calibration. The technician must connect standard DC voltage levels to the input connectors. The scope then automatically calibrates the vertical input attenuators' gain and the external trigger amplifier's gain and offset using the supplied dc voltages. During the ATTEN calibration, the accuracy of the internal 10-V Calibration Reference is verified against the standard amplitude voltage applied to the attenuators.

The EXT CAL routines also provide automatic REPET calibration and the display signals for the manual adjustments needed for the Display System and CCD output amplifier calibrations. REPET calibration adjusts the timing of the jitter correction ramps. The jitter correction ramps are used to measure the time between the randomly acquired samples and the trigger point. That time difference is used to place the waveform samples correctly with respect to the trigger point in the repetitive acquisition mode waveform record.

Manual Adjustments

Adjustments requiring internal access to the scope are limited to the display system, CCD output amplifier gains, input capacitance, 100 MHz bandwidth limiter (and 20 MHz bandwidth limiter with the Video Option), CCD clocks, and transient response. These adjustments are made during factory calibration and should not require readjustment during normal operation. Replacement of parts during repair of the instrument that affect these calibrations will, however, require readjustment of the affected circuitry. The ADJUSTS calibration routine in the EXTENDED CALIBRATION procedures provides display patterns and brief instructions for the technician to follow in calibrating the display system and CCD output amplifier gains.

Dynamic Adjustments

As the instrument operates, it continuously corrects for minor offsets in the acquisition system and jitter correction ramp timing. These "dynamic" adjustments are totally automatic and require no user action.

Recommended Adjustment Intervals

Perform the ATTEN and TRIGGER parts of the Extended Calibration procedure every 2000 hours, or once a year if the instrument is used infrequently. Readjustment of the Display System and rerunning the REPET calibration step is not normally needed unless parts are replaced that affect those calibrations. It is NOT necessary to reperform any portion of the Extended Calibration to maintain maximum measurement accuracy over the specified operating temperature range of the instrument.

NATIONAL BUREAU OF STANDARDS TRACEABILITY

Traceability to the National Bureau of Standards (NBS) requires that the stated accuracy of an instrument be established by calibration with equipment whose accuracies have been directly or indirectly established by NBS certified references.

For this oscilloscope, traceability is established in the Extended Calibration routine by calibrating the attenuators (ATTEN) and external trigger amplifiers (TRIGGER) with an NBS traceable voltage reference. As the fine gain adjustment of the attenuators is made, the relative accuracy of the internal 10-V Calibration Reference is also checked by normalizing it to the external voltage source provided by the technician. If the fine gain of the attenuators requires an adjustment of more than approximately 2%, the ATTEN calibration fails. Barring internal component problems, a failure indicates either that the internal reference is faulty or that the applied voltage is not a valid standard reference voltage.

Passing the ATTEN calibration step using an NBS traceable voltage standard ensures that the internal, nonadjustable 10-V Calibration Reference is also traceable. Subsequently passing the SELF CAL procedure (which uses the traceable 10-V Calibration Reference to provide the calibration voltages) then makes this scope an NBS traceable instrument. Traceability is maintained for subsequent performances of SELF CAL by referencing all calibration calculations to the traceable internal voltage reference.

VOIDING CALIBRATION

Factory calibration of this scope is done using NBS traceable sources. An internal jumper installed at the time of calibration prevents the user from inadvertently running the EXT CAL routines and voiding the traceable calibration of the instrument. Removing the jumper and attempting to do the ATTEN and TRIGGER calibration without an accurate standard amplitude voltage source will result in a failed calibration. In the case of a failure, the stored constants for the attenuator gain calibration are not replaced; therefore, the previous degree of accuracy is maintained by the instrument. However, a FAIL label remains displayed over the affected EXT CAL menu choice, and the scope will fail subsequent power-on tests and enter Extended Diagnostics (EXT DIAG) until the calibration is passed.

Power-on or Self Diagnostics (SELF DIAG) tests that detect a system, subsystem, or device failure that may affect instrument calibration are noted by a FAIL label on the test along with the calibration status of UNCALD in the EXT DIAG menu display. Calibration failures are of two types: soft errors caused by gain or offset parameter drifts beyond tolerance—usually caused by a large change in

operating temperature since the last SELF CAL was done, or hard failures caused by component problems in the instrument's circuitry that prevent calibration.

Soft Errors

These errors appear as a loss of SELF CAL and are noted by the UNCALD label appearing above the SELF CAL choice in the main CAL/DIAG menu. Running the SELF CAL routine and obtaining a PASS status clears up any soft calibration errors and revalidates the instrument calibration.

Hard Failures

A hard failure affecting calibration may also be indicated by the loss of SELF CAL, but running the SELF CAL routine does not produce a PASS status for SELF CAL or any failed test in EXT DIAG. Loss of ATTEN or external TRIGGER calibration is noted by the UNCALD label appearing above those choices in the EXT CAL menu. A loss of calibration for either ATTEN or TRIGGER indicates a possible nonvolatile memory failure. In either case, instrument calibration should be considered void, and the scope must be referred to a qualified service person for servicing.

STATIC-SENSITIVE COMPONENTS

The following precautions apply when performing any maintenance involving internal access to the instrument.



Static discharge can damage any semiconductor component in this instrument.

This instrument contains electrical components that are susceptible to damage from static discharge. Table 6-1 lists the relative susceptibility of various classes of semiconductors. Static voltages of 1 kV to 30 kV are common in unprotected environments.

When performing maintenance, observe the following precautions to avoid component damage:

- 1. Minimize handling of static-sensitive components.
- 2. Transport and store static-sensitive components or assemblies in their original containers or on a metal rail. Label any package that contains static-sensitive components or assemblies.
- 3. Discharge the static voltage from your body by wearing a grounded antistatic wrist strap while handling these components. Servicing static-sensitive components or assemblies should be performed only at a static-free work station by qualified service personnel.
- 4. Nothing capable of generating or holding a static charge should be allowed on the work station surface.

- 5. Keep the component leads shorted together whenever possible.
- 6. Pick up components by their bodies, never by their leads.

Table 6-1

Relative Susceptibility to Static-Discharge Damage

Semiconductor Classes	Relative Susceptibility Levels ^a				
MOS or CMOS microcircuits or discretes, or linear microcircuits with MOS inputs (Most Sensitive)	1				
ECL	2				
Schottky signal diodes	3				
Schottky TTL	4				
High-frequency bipolar transistors	5				
JFET	6				
Linear microcircuits	7				
Low-power Schottky TTL	8				
TTL (Least Sensitive)	9				

^aVoltage equivalent for levels (voltage discharged from a 100 pF capacitor through a resistance of 100 ohms):

1 = 100 to 500 V 4 = 500 V 7 = 400 to 1000 V (est)

2 = 200 to 500 V 5 = 400 to 600 V 8 = 900 V

3 = 250 V 6 = 600 to 800 V 9 = 1200 V

- 7. Do not slide the components over any surface.
- 8. Avoid handling components in areas that have a floor or work-surface covering capable of generating a static charge.
- 9. Use a soldering iron that is connected to earth ground.
- 10. Use only approved antistatic, vacuum-type desoldering tools for component removal.

PREVENTIVE MAINTENANCE

INTRODUCTION

Preventive maintenance consists of cleaning, visual inspection, and checking instrument performance. When performed regularly, it may prevent instrument malfunction and enhance instrument reliability. The severity of the environment in which the instrument is used determines the required frequency of maintenance. An appropriate time to perform preventive maintenance is just before instrument adjustment.

GENERAL CARE

The cabinet minimizes accumulation of dust inside the instrument and should normally be in place when operating the oscilloscope. The instrument's front cover protects the front panel and crt from dust and damage. It should be installed whenever the instrument is stored or transported.

INSPECTION AND CLEANING

The scope should be visually inspected and cleaned as often as operating conditions require. Accumulation of dirt in the instrument can cause overheating and component breakdown. Dirt on components acts as an insulating blanket, preventing efficient heat dissipation. It also provides an electrical conduction path that could result in instrument failure, especially under high-humidity conditions.

CAUTION

Avoid the use of chemical cleaning agents which might damage the plastics used in this instrument. Use a nonresidue-type cleaner, preferably isopropyl alcohol or a solution of 1% mild detergent with 99% water. Before using any other type of cleaner, consult your Tektronix Service Center or representative.

Exterior

INSPECTION. Inspect the external portions of the instrument for damage, wear, and missing parts; use Table 6-2 as a guide. Instruments that appear to have been dropped or otherwise abused should be checked thoroughly to verify correct operation and performance. Repair deficiencies that could cause personal injury or lead to further damage to the instrument immediately.



To prevent getting moisture inside the instrument during external cleaning, use only enough liquid to dampen the cloth or applicator.

CLEANING. Loose dust on the outside of the instrument can be removed with a soft cloth or small soft-bristle brush. The brush is particularly useful for dislodging dirt on and around the controls and connectors. Dirt that remains can be removed with a soft cloth dampened in a mild detergent-and-water solution. Do not use abrasive cleaners.

Two plastic light filters, one blue and one clear, are provided with the oscilloscope. Clean the light filters and the crt face with a soft lint-free cloth dampened with either isopropyl alcohol or a mild detergent-and-water solution.

Interior

To access the inside of the instrument for inspection and cleaning, refer to the "Removal and Replacement Procedure" in the "Corrective Maintenance" part of this section.

INSPECTION. Inspect the internal portions of the scope for damage and wear, using Table 6-3 as a guide. Deficiencies found should be repaired immediately. The

corrective procedure for most visible defects is obvious; however, particular care must be taken if heat-damaged components are found. Overheating usually indicates other trouble in the instrument; it is important, therefore, that the cause of overheating be corrected to prevent recurrence of the damage.

If any electrical component is replaced, conduct a Performance Check for the affected circuit and for other closely related circuits (see Section 4). If repair or replacement work is done on any of the power supplies, verify that the affected power supply meets the voltage and ripple tolerance requirements under Specification in Section 1 of this manual.

CAUTION

To prevent damage from electrical arcing, ensure that circuit boards and components are dry before applying power to the instrument.

CLEANING. To clean the interior, blow off dust with dry, low-pressure air (approximately 9 psi). Remove any remaining dust with a soft brush or a cloth dampened with a solution of mild detergent and water. A cotton-tipped applicator is useful for cleaning in narrow spaces and on circuit boards. If these methods do not remove all the dust or dirt, the instrument may be spray washed using a solution of 5% mild detergent and 95% water as follows:

CAUTION

Exceptions to the following cleaning procedure are the CH 1 and CH 2 Attenuator assemblies. Clean these assemblies only with isopropyl alcohol as described in Step 4 of the cleaning procedure. In addition, all other Front Panel controls are sealed and require no maintenance.

- 1. Gain access to the parts to be cleaned by removing easily accessible shields and panels (see "Removal and Replacement Procedure").
- 2. Spray wash dirty parts with the detergent-and-water solution; then use clean water to thoroughly rinse them.
 - 3. Dry all parts with low-pressure air.
- 4. Clean switches with isopropyl alcohol and wait 60 seconds for the majority of the alcohol to evaporate. Then complete drying with low-pressure air.
- 5. Dry all components and assemblies in an oven or drying compartment using low-temperature (125°F to 150°F) circulating air.

Table 6-2
External Inspection Check List

Item	Inspect For	Repair Action
Cabinet, Front Panel, and Cover	Cracks, scratches, deformations, damaged hardware or gaskets.	Touch up paint scratches and replace defective components.
Front-panel Controls	Missing, damaged, or loose knobs, buttons, and controls.	Repair or replace missing or defective items.
Connectors	Broken shells, cracked insulation, and deformed contacts. Dirt in connectors.	Replace defective parts. Clear or wash out dirt.
Carrying Handle	Correct operation.	Replace defective parts.
Accessories	Missing items or parts of items, bent pins, broken or frayed cables, and damaged connectors.	Replace damaged or missing items, frayed cables, and defective parts.

Table 6-3 Internal Inspection Check List

item	Inspect For	Repair Action				
Circuit Boards	Loose, broken, or corroded solder connections. Burned circuit boards. Burned, broken, or cracked circuit-run plating.	Clean solder corrosion with an eraser and flush with isopropyl alcohol. Resolder defective connections. Determine cause or burned items and repair. Repair defective circuit runs.				
Resistors	Burned, cracked, broken, blistered.	Replace defective resistors. Check for cause of burned component and repair as necessary.				
Solder Connections	Cold solder or rosin joints.	Resolder joint and clean with isopropyl alcohol.				
Capacitors	Damaged or leaking cases. Corroded solder on leads or terminals.	Replace defective capacitors. Clean solder connections and flush with isopropyl alcohol.				
Semiconductors	Loosely inserted in sockets. Distorted pins.	Firmly seat loose semiconductors. Remove devices having distorted pins. Carefully straighten pins (as required to fit the socket), using long-nose pliers, and reinsert firmly. Ensure that straightening action does not crack pins, causing them to break off.				
Wiring and Cables	Loose plugs or connectors. Burned, broken, or frayed wiring.	Firmly seat connectors. Repair or replace defective wires or cables.				
Chassis	Dents, deformations, and damaged hardware.	Straighten, repair, or replace defective hardware.				

LUBRICATION

There is no periodic lubrication required for this instrument,

SEMICONDUCTOR CHECKS

Periodic checks of the transistors and other semiconductors in the oscilloscope are not recommended. The best check of semiconductor performance is actual operation in the instrument.

PERIODIC READJUSTMENT

To ensure accurate measurements, check the performance of this instrument every 2000 hours of operation, or if used infrequently, once each year. In addition, replacement of components may necessitate readjustment of the affected circuits.

Complete Performance Check and Adjustment procedures are given in Sections 4 and 5. The Performance Check Procedure can also be helpful in localizing certain troubles in the instrument. In some cases, minor problems may be revealed or corrected by readjustment.

TROUBLESHOOTING

INTRODUCTION

Preventive maintenance performed on a regular basis should reveal most potential problems before an instrument malfunctions. However, should troubleshooting be required, the following information is provided to facilitate location of a fault. In addition, the material presented in the "Theory of Operation" and "Diagrams" sections of this manual may be helpful while troubleshooting.

TROUBLESHOOTING AIDS

Diagnostic Firmware

The operating firmware in this instrument contains diagnostic routines that aid in locating malfunctions. When instrument power is applied, power-up tests are performed to verify proper operation of the instrument. If a failure is detected, this information is passed on to the operator in the form of a CRT readout error message. The failure information directs the troubleshooter to the area of failing circuitry. If the failure is such that the processor can still execute the diagnostic routines, the user can call up specific tests to further check the failing circuitry. The specific diagnostic routines are explained later in this section.

Schematic Diagrams

Complete schematic diagrams are located on tabbed foldout pages in the "Diagrams" section. Heavy black lines that enclose portions of the circuitry represent the circuit board on which the enclosed circuitry is mounted. The assembly number and name of the circuit board are shown near either the top or the bottom edge of the diagram.

Functional blocks on schematic diagrams are outlined with a wide grey line. Components within the outlined area perform the function designated by the block label. The "Detailed Block Diagram Description" in the "Theory of Operation" uses these functional block names when describing circuit operation, aiding in cross-referencing between the two circuit descriptions and the schematic diagrams.

Component numbers and electrical values of components in this instrument are shown on the schematic diagrams. Refer to the first page of the "Diagrams" section for the reference designators and symbols used to identify components. Important voltages and waveform reference numbers (enclosed in hexagonally-shaped boxes) are also shown on each diagram. Waveform illustrations are located adjacent to their respective schematic diagram.

Circuit Board Illustrations

Circuit board illustrations showing the physical location of each component are provided for use in conjunction with each schematic diagram. Each board illustration is found in the "Diagrams" section on the back of a foldout page, preceding the first schematic diagram(s) to which it relates.

The locations of waveform test points are marked on the circuit board illustrations with hexagonally outlined numbers corresponding to the waveform numbers on both the schematic diagram and the waveform illustrations.

Circuit Board Locations

The placement of each circuit board in the instrument is shown in a board locator illustration. This illustration is located on the foldout page along with the circuit board illustration.

Circuit Board Interconnections

A circuit board interconnection diagram is provided in the "Diagrams" section to aid in tracing a signal path or power source between boards. All wire, plug, and jack numbers are shown along with their associated wire or pin numbers.

Power Distribution

Power distribution is traceable through the schematic diagrams in the "Diagrams" section. The low-voltage power supplies originate on the Power Supply board and are schematically illustrated in diagrams 22 and 23. The high-voltage and +61 V power supplies, originating on the High Voltage board, are shown in diagram 19. Any power supply can be tracked back to its diagram and forward to other circuitry illustrated on different diagrams.

Power is distributed to the different circuit boards through interconnect assemblies consisting of one or more connectors. The diagrams showing these assemblies (or partial assemblies) provide the interconnecting assembly (wire, plug, and/or jack) numbers, as well as the number

for the individual pins or wires distributing the supplies. By referencing the numbers for the assembly and its connector wire(s), the diagram showing that section of the power distribution path immediately preceding the section illustrated (on a given diagram) can be determined.

If power is carried to another interconnect assembly and on to another circuit board, that distribution is shown. The other interconnect assembly and conductors are labeled as previous described, except the an individual connector number indicates the diagram showing the succeeding distribution path section rather than the preceding section. This method allows the tracing of power distribution either up the path towards the originating supply, or away (further down the distribution path) from that supply.

In some cases, the diagram showing an interconnect assembly carrying power to a circuit board may not illustrate all of that circuit board. Arrows pointing to diagram numbers indicate other schematic diagrams (illustrating other parts of the circuit board) where the supplies are routed. Further, any diagram showing a partial circuit board will indicate the number of the diagram where the interconnect assembly(ies) routing power supplies to that board is illustrated. This method allows tracing power distribution back to an interconnect assembly, at which point further distribution tracing can occur.

As a further aid to power supply distribution, the "Diagrams" section contains an interconnect diagram. This diagram shows all of the interconnections between the various circuit board assemblies, including the power supplies. This diagram can also be an aid in power distribution tracing.

Grid Coordinate System

Each schematic diagram and circuit board illustration has a grid border along its left and top edges. A table located adjacent to each diagram lists the grid coordinates of each component shown on that diagram. To aid in physically locating components on the circuit board, this table also lists the grid coordinates of each component on the circuit board illustration.

Near each circuit board illustration is an alphanumeric listing of all components mounted on that board. The second column in each listing identifies the schematic diagram in which each component can be found. These component-locator tables are especially useful when more than one schematic diagram is associated with a particular circuit board.

Troubleshooting Charts

The troubleshooting charts contained in the "Diagrams" section are to be used in conjunction with the Extended Diagnostics of Table 6-6 (at the back of this section) as an aid in locating malfunctioning circuitry. To use the charts, begin with the Initial Troubleshooting Guide shown in Figure 6-6. This guide will help identify problem areas and will direct you to the appropriate procedures for further troubleshooting.

Component Color Coding

Information regarding color codes and markings of resistors and capacitors is located on the color-coding illustration (Figure 9-1) at the beginning of the "Diagrams" section.

Semiconductor Lead Configurations

Figure 9-2 in the "Diagrams" section shows the lead configurations for most types of semiconductor devices used in the instrument. Vendor changes and performance improvement changes may result in changes of case styles or lead configurations. If the device in question does not appear to match a configuration shown in Figure 9-2, examine the associated circuitry or consult a manufacturer's data sheet to obtain the pin nomenclature.

Multipin Connectors

Multipin connector orientation is indexed by two triangles; one on the holder and one on the circuit board. Slot numbers are usually molded into the holder. When a connection is made to circuit board pins, ensure that the index on the holder is aligned with the index on the circuit board (see Figure 6-1).

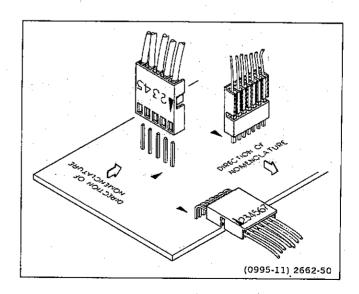


Figure 6-1. Multipin connector.

TROUBLESHOOTING EQUIPMENT

The equipment listed in Table 4-1 of this manual, or equivalent equipment, may be useful when troubleshooting this instrument.

TROUBLESHOOTING TECHNIQUES

In the following list of troubleshooting procedures, the first two steps use diagnostic aids inherent in the instrument's operating firmware. These built-in tests can locate many circuit faults to aid in isolating the problem circuitry. The next four procedures are check steps that ensure proper control settings, connections, operation, and adjustment. If the trouble is not located by these checks, the remaining steps will aid in locating the defective component. When the defective component is located, replace it using the appropriate replacement procedure given under "Corrective Maintenance" in this section.

CAUTION

Before using any test equipment to make measurements on static-sensitive, current-sensitive, or voltage-sensitive components or assemblies, ensure that any voltage or current supplied by the test equipment does not exceed the limits of the component to be tested.

1. Power-up Tests

This scope performs automatic verification of the instrument. If a failure occurs, refer to the "Calibration and Diagnostics" discussion later in this section for interpreting the failure.

If a problem is found, the associated troubleshooting procedure may be used to isolate the problem. The troubleshooting procedures are found in Table 6-6 (located in the "Diagnostics" subsection). See Figure 6-6 (also in the Diagnostics subsection) for the Initial Troubleshooting Guide.

2. Diagnostic Test Routines.

The instrument firmware contains diagnostic routines that may be selected by the user from the front panel to further clarify the nature of a suspected failure. The desired test is selected using the MENU buttons after entering the Extended Diagnostics Mode. Entry into the Diagnostic Mode and its uses are explained in the "Calibration and Diagnostics" discussion later in this section.

3. Check Control Settings

Incorrect control settings can give a false indication of instrument malfunction. If there is any question about the correct function or operation of any control, refer to either the "Operating Information" in Section 2 of this manual or to the scope's Operators Manual.

4. Check Associated Equipment

Before proceeding, ensure that any equipment used with the scope is operating correctly. Verify that input signals are properly connected and that the interconnecting cables are not defective. Check that the ac-power-source voltage to all equipment is correct.

5. Visual Check

WARNING

To avoid electrical shock, disconnect the instrument from the ac power source before making a visual inspection of the internal circuitry.

Perform a visual inspection. This check may reveal broken connections or wires, damaged components, semiconductors not firmly mounted, damaged circuit boards, or other clues to the cause of an instrument malfunction.

Check Instrument Performance and Adjustment

Check the performance of those areas where trouble appears to exist. The trouble condition observed may be the result of a lack of calibration. Complete Performance Check and Adjustment procedures are given in Sections 4 and 5 of this manual respectively.

7. Isolate Trouble to a Circuit

To isolate problems to a particular area, use any symptoms noticed to help locate the trouble. Refer to the Extended Diagnostics table (Table 6-6) in the "Calibration and Diagnostics" discussion in this section as an aid in locating a faulty circuit.

8. Check Power Supplies

WARNING

For safety reasons, an isolation transformer must be connected whenever troubleshooting in the Preregulator and Inverter Power Supply sections of the instrument. When trouble symptoms appear in more than one circuit, first check the power supplies; then check the affected circuits by taking voltage and waveform readings. Check first for the correct output voltage of each individual supply; then measure ac ripple to check that it is within the Total Peak-to-Peak Ripple specification. Table 6-4 lists the power supply voltage level and ripple limits for each supply.

These voltages are measured between the power supply test points (most of which are located on the Side Board near the Front Panel μ P) and ground. Voltage ripple amplitudes must be measured using an oscilloscope. Before measuring ac ripple, set the STORAGE ACQUIRE mode of the 2440 to SAVE. Use a 1X probe having as short a ground lead as possible to minimize stray pickup.

NOTE

The oscilloscope used to measure ripple must be bandwidth limited to 20 MHz. Use of a higher bandwidth oscilloscope without 20 MHz bandwidth limiting will result in higher readings.

Table 6-4

Power Supply Voltage and Ripple Limits^a

Power Supply	Reading → (Volts)	P-P Ripple (mV)		
+61 V	59.05 to 62.95	100		
+15 V	14.74 to 15.26	10		
+10 V Ref	9.97 to 10.03	10		
+8 V	7.85 to 8.15	10		
+5 V	4.91 to 5.09	10		
+5 VD (digital)	4.83 to 5.17	150		
_5 V	-4.95 to -5.05	10		
-8 V	-7.85 to -8.15	10		
–15 V	-14.74 to -15.26	10		
-15 V unreg		350		
-1900 V	-1855 to -1945			

aAt 25°C.

If the power-supply voltages and ripple are within the listed ranges in Table 6-4, the supply can be assumed to be working correctly. If the supply is not within specified ranges, the fault may or may not be located in the power supply circuitry. A defective component elsewhere in the instrument can create the appearance of a power-supply problem and may also affect the operation of other circuits. Use the power supply troubleshooting charts to aid in locating the problem.

9. Check Circuit Board Interconnections

After the trouble has been isolated to a particular circuit, again check for loose or broken connections, improperly seated semiconductors, and heat-damaged components.

10. Check Voltages and Waveforms

Often the defective component can be located by checking circuit voltages or waveforms. Typical voltages are listed on the schematic diagrams. Waveforms indicated on the schematic diagrams by hexagonally outlined numbers are shown adjacent to the diagrams. Waveform test points are shown on the circuit board illustrations.

NOTE

Voltages and waveforms indicated on the schematic diagrams are not absolute and may vary slightly between instruments. To establish operating conditions similar to those used to obtain these readings, set up the Test scope and the 2440 under test as indicated near the waveform illustrations for a schematic diagram.

11. Check Individual Components

WARNING

To avoid electric shock, always disconnect the instrument from the ac power source before removing or replacing components.

CAUTION

When checking semiconductors, observe the staticsensitivity precautions located at the beginning of this section. To accurately check components, it is often necessary to remove or partially disconnect the component from the circuit board, in order to isolate it from surrounding circuitry. Partial specifications (resistor tolerance, transistor type, etc.) for most components can be found by referencing the component designation number in the "Replaceable Electrical Parts." Also see Figure 9-1 for component value identification and Figure 9-2 for semiconductor lead configurations.

12. Repair and Adjust the Circuit

If any defective parts are located, follow the replacement procedures given under "Corrective Maintenance" in this section. After any electrical component has been replaced, the performance of that circuit and any other closely related circuit should be checked. If work has been done on the power supplies, a complete check of the regulated voltages should be done to verify that the supply voltages are in tolerance. A check of the Display ADJUSTS calibration and a SELF CAL should verify that the instrument meets Performance Requirements if the voltages are all correct.

CORRECTIVE MAINTENANCE

INTRODUCTION

Corrective maintenance consists of component replacement and instrument repair. This part of the manual describes special techniques and procedures required to replace components in this instrument. If it is necessary to ship your instrument to a Tektronix Service Center for repair or service, refer to the "Repackaging for Shipment" information in Section 2 of this manual.

- 3. Use care not to interconnect instrument grounds which may be at different potentials (cross grounding).
- 4. When soldering on circuit boards or small insulated wires, use only a 15-watt, pencil-type soldering iron.
- 5. Use an isolation transformer to supply power to the 2440 if removing the shield and troubleshooting in the power supply.

MAINTENANCE PRECAUTIONS

To reduce the possibility of personal injury or instrument damage, observe the following precautions:

- Disconnect the instrument from the ac-power source before removing or installing components.
- 2. Verify that the line-rectifier filter capacitors are discharged prior to performing any servicing.

OBTAINING REPLACEMENT PARTS

Most electrical and mechanical parts can be obtained through your local Tektronix Field Office or representative. However, many of the standard electronic components can usually be obtained from a local commercial source. Before purchasing or ordering a part from a source other than Tektronix, Inc., please check the "Replaceable Electrical Parts" list for the proper value, rating, tolerance, and description.

NOTE

Physical size and shape of a component may affect instrument performance, particularly at high frequencies. Always use direct-replacement components, unless it is known that a substitute will not degrade instrument performance.

Special Parts

In addition to the standard electronic components, many special parts are used in this scope. These components are manufactured or selected by Tektronix, Inc. to meet specific performance requirements, or are manufactured for Tektronix, Inc. in accordance with our specifications. The various manufacturers can be identified by referring to the "Cross Index—MFR Code Number to Manufacturer" at the beginning of the "Replaceable Electrical Parts" list. Most of the mechanical parts used in this instrument were manufactured by Tektronix, Inc. Order all special parts directly from your local Tektronix Field Office or representative.

Ordering Parts

When ordering replacement parts from Tektronix, Inc., be sure to include all of the following information:

- Instrument type (include modification or option numbers).
- 2. Instrument serial number.
- A description of the part (if electrical, include its full circuit component number).
- 4. Tektronix part number.

MAINTENANCE AIDS

The maintenance aids listed in Table 6-5 include items required for performing most of the maintenance procedures in this instrument. Equivalent products may be substituted for the examples given, provided their characteristics are similar.

INTERCONNECTIONS

Interconnections in this instrument are made with pins soldered onto the circuit boards. Several types of mating

connectors are used for the interconnecting pins. The following information provides the replacement procedures for the various types of connectors.

End-Lead Pin Connectors

Pin connectors used to connect the wires to the interconnect pins are factory assembled. They consist of machine-inserted pin connectors mounted in plastic holders. If the connectors are faulty, the entire wire assembly should be replaced.

Multipin Connectors

When pin connectors are grouped together and mounted in a plastic holder, they are removed, reinstalled, or replaced as a unit. If any individual wire or connector in the assembly is faulty, the entire cable assembly should be replaced. To provide correct orientation of a multipin connector, an index arrow is stamped on the circuit board, and either a matching arrow is molded into or the numeral 1 is marked on the plastic housing as a matching index. Be sure these index marks are aligned with each other when the multipin connector is reinstalled.

TRANSISTORS AND INTEGRATED CIRCUITS

Transistors and integrated circuits should not be replaced unless they are actually defective. If removed from their sockets or unsoldered from the circuit board during routine maintenance, return them to their original board locations. Unnecessary replacement or transposing of semiconductor devices may affect the adjustment of the instrument. When a semiconductor is replaced, check the performance of any circuit that may be affected.

Any replacement component should be of the original type or a direct replacement. Bend transistor leads to fit their circuit board holes, and cut the leads to the same length as the original component. See Figure 9-2 in the "Diagrams" section for lead-configuration illustrations.

CAUTION

After replacing a power transistor, check that the collector is not shorted to the chassis before applying power to the instrument.

Table 6-5
Maintenance Aids

Description	Specification	Usage	Example Antex Precision Model C.				
1. Soldering Iron	15 to 25 W.	General soldering and unsoldering.					
2. Torx Screwdrivers	Torx tips #T7, #T9, #T10, #T15, and #T20.	Assembly and disassembly.	Tektronix Part Numbers: 003-1293-00 003-0965-00 003-0814-00 003-0966-00 003-0866-00.				
3. Nutdrivers	1/4 inch, 7/32 inch, 5/16 inch, 1/2 inch, and 9/16 inch.	Assembly and disassembly.	Xcelite #7, #8, #10, #16, and #18.				
4. Open-end Wrench	9/16 inch and 1/2 inch.	Channel Input and Ext Trig BNC Connectors.	Tektronix Part Numbers: 9/16 in. 003-0502-00 1/2 in. 003-0882-00.				
5. Hex Wrenches	0.050 inch, 1/16 inch.	Assembly and disassembly.	Allen Wrenches.				
6. Long-nose Pliers		Component removal and replacement.	Diamalloy Model LN55-3.				
7. Diagonal Cutters		Component removal and replacement.	Diamalloy Model M554-3.				
8. Vacuum Solder Extractor	No static charge retention.	Unsoldering static sensitive devices and components on multilayer boards.	Pace Model PC-10.				
Contact Cleaner and lubricant	No-Noise R.	Switch and pot cleaning and lubrication.	Tektronix Part Number: 006-0442-02.				
10. Pin-Replacement Kit		Replace circuit board con- nector pins.	Tektronix Part Number: 040-0542-00.				
11. IC-Removal Tool		Removing DIP IC packages.	Augat T114-1.				
12. Isopropyl Alcohol	Reagent grade.	Cleaning attenuator and front-panel assemblies.	2-Isopropanol.				
13. Isolation Transformer ^a		Isolate the instrument from the ac power source for safety.	Tektronix Part Number 006-5953-00.				
14. 1X Probe		Power supply ripple check.	TEKTRONIX P6101 Probe (1X) Part Number 010-6101 03.				

^aThe isolation transformer (item 13) is an important SAFETY item. The switching power supply of the scope has areas that float at the ac-source potential, and a serious shock hazard exists when the power supply safety shield is removed to permit trouble-shooting if power is applied directly from the ac-source.

Maintenance-2440 Service

The chassis-mounted power supply transistor is insulated from the chassis by a heat-transferring mounting block. Reinstall the mounting block and bushings when replacing these transistors. Use a thin layer of heat-transferring compound between the insulating block and chassis when reinstalling the block.

To remove socketed dual-in-line packaged (DIP) integrated circuits, pull slowly and evenly on both ends of the device. Avoid disengaging one end of the integrated circuit from the socket before the other, since this may damage the pins.

To remove a soldered DIP IC when it is going to be replaced, clip all the leads of the device and remove the leads from the circuit board one at a time. If the device must be removed intact for possible reinstallation, do not heat adjacent conductors consecutively. Apply heat to pins at alternate sides and ends of the IC as solder is removed. Allow a moment for the circuit board to cool before proceeding to the next pin.

SOLDERING TECHNIQUES

The reliability and accuracy of this instrument can be maintained only if proper soldering techniques are used to remove or replace parts. General soldering techniques, which apply to maintenance of any precision electronic equipment, should be used when working on this instrument.

WARNING

To avoid an electric-shock hazard, observe the following precautions before attempting any soldering: turn the instrument off, disconnect it from the ac power source, and wait at least three minutes for the line-rectifier filter capacitors to discharge. Use rosin-core wire solder containing 63% tin and 37% lead. Contact your local Tektronix Field Office or representative to obtain the names of approved solder types.

When soldering on circuit boards or small insulated wires, use only a 15-watt, pencil-type soldering iron. A higher wattage soldering iron may cause etched circuit conductors to separate from the board base material and melt the insulation on small wires. Always keep the soldering-iron tip properly tinned to ensure best heat transfer from the iron tip to the solder joint. Apply only enough solder to make a firm joint. After soldering, clean the area around the solder connection with an approved flux-removing solvent (such as isopropyl alcohol) and allow it to air dry.

CAUTION

Only an experienced maintenance person, proficient in the use of vacuum-type desoldering equipment should attempt repair of any circuit board in this instrument. Many integrated circuits are static sensitive and may be damaged by solder extractors that generate static charges. Perform work involving static-sensitive devices only at a static-free work station while wearing a grounded antistatic wrist strap. Use only an antistatic vacuum-type solder extractor approved by a Tektronix Service Center.

CAUTION

Attempts to unsolder, remove, and resolder leads from the component side of a circuit board may cause damage to the reverse side of the circuit board.

The following techniques should be used to replace a component on a circuit board:

1. Touch the vacuum desoldering tool to the lead at the solder connection. Never place the iron directly on the board; doing so may damage the board.

NOTE

Some components are difficult to remove from the circuit board due to a bend placed in the component leads during machine insertion. To make removal of machine-inserted components easier, straighten the component leads on the reverse side of the circuit board.

2. When removing a multipin component, especially an IC, do not heat adjacent pins consecutively. Apply heat to the pins at alternate sides and ends of the IC as solder is removed. Allow a moment for the circuit board to cool before proceeding to the next pin.

CAUTION

Excessive heat can cause the etched circuit conductors to separate from the circuit board. Never allow the solder extractor tip to remain at one place on the board for more than three seconds. Solder wick, spring-actuated or squeeze-bulb solder suckers, and heat blocks (for desoldering multipin components) must not be used. Damage caused by poor soldering techniques can void the instrument warranty.

- 3. Bend the leads of the replacement component to fit the holes in the circuit board. If the component is replaced while the board is installed in the instrument, cut the leads so they protrude only a small amount through the reverse side of the circuit board. Excess lead length may cause shorting to other conductive parts.
- 4. Insert the leads into the holes of the board so that the replacement component is positioned the same as the original component. Most components should be firmly seated against the circuit board.
- 5. Touch the soldering iron to the connection and apply enough solder to make a firm solder joint. Do not move the component while the solder hardens.

- 6. Cut off any excess lead protruding through the circuit board (if not clipped to the correct length in Step 3).
- 7. Clean the area around the solder connection with an approved flux-removing solvent. Be careful not to remove any of the printed information from the circuit board.

REMOVAL AND REPLACEMENT PROCEDURE

Read these instructions completely before attempting any corrective maintenance.

WARNING

To avoid electric shock, disconnect the instrument from the ac power source before removing or replacing any component or assembly.

The exploded view drawing in the "Replaceable Mechanical Parts" list at the rear of this manual may be helpful during the removal and installation of individual components or subassemblies. Figure 6-2 illustrates the locations of the circuit boards referred to in this procedure. Individual circuit boards are illustrated in the "Diagrams" section of this manual; those illustrations are useful in location of the components referred to in this procedure.

As a further aid in component location, this procedure specifies the location of most of the components to be disconnected. The component side of a circuit board is referred to as the "top" side of the board; the edge nearest the Front Panel is the front edge. The remaining sides and edges follow from this orientation.

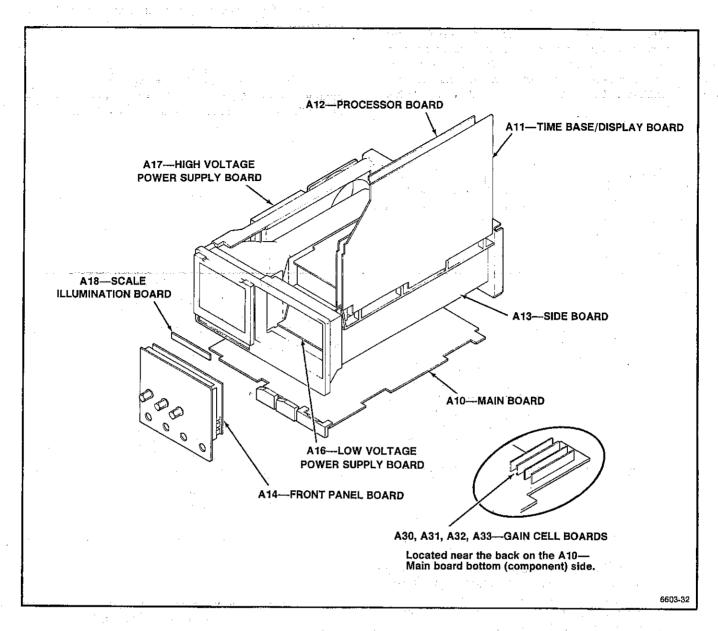


Figure 6-2. Circuit Board Location.

1. Cabinet Removal

- a. Disconnect the power cord from any ac power source.
- b. Disconnect the power cord from its receptacle at the instrument's Rear panel.
- c. Grasp the power cord plug (female end), rotate the power cord retainer 1/4 turn, and pull it to remove the cord from the Rear panel.
- d. Grasp the handle hubs (at right and left side of the instrument) and pull outward. Rotate the hubs to position the front of the handle away from the front of the instrument.
- e. Install the protective Front cover over the Front panel. Push on the cover to lock the cover's side tabs around the Front panel's trim band.
 - f. Set the instrument so it rests on the Front cover.
- g. Remove the four screws inside the four rear feet at the instrument's back panel.

WARNING

Dangerous potentials exist at several points throughout this instrument. If it is operated with the cabinet removed, do not touch exposed connections or components. Some transistors may have elevated case voltages. Disconnect the ac power source from the instrument and verify that the line-rectifier filter capacitors have discharged before cleaning the instrument or replacing parts (see label on the Low Voltage Power Supply cover).

h. Grasp the handle hubs (at right and left sides of the instrument) and pull outward. While holding the hubs outward, pull straight up from the rear of the cabinet to remove the cabinet from the instrument.

Reverse parts a through h to install the cabinet.

WARNING

The line-rectifier capacitors normally retain a charge for several minutes after the instrument is powered off and can remain charged for a longer period if a bleeder resistor or other power supply problem occurs. Before beginning any cleaning or work on the internal circuitry of the instrument, discharge the capacitors by connecting a shorting strap in series with a $1~\mathrm{k}\Omega$, $5~\mathrm{watt}$ resistor across the capacitors. Connect one end of the shorting strap/resistor combination to upper-most terminal of S1020 (the terminal connected through a wire to W310). Connect the other end to pin 11 of T117 (the pin protruding from the side of the transformer, near its right-rear corner). Measure across those two connections with a voltmeter to ensure the capacitors are discharged.

2. Timebase/Display Board Removal

- a. Perform Step 1 to remove the cabinet.
- b. Set the instrument on a flat, smooth surface, with its underside facing down and the Front panel facing forward.
- c. Disconnect the ribbon-cable connector from J100 of the Timebase/Display board. J100 is located at the rightfront corner of the Timebase/Display board.
- d. Disconnect the ribbon cable connector at J141 of the Main board. J141 is located at the lower right-rear corner of the instrument.
- e. Disconnect the ribbon cable connector at J121 of the Timebase/Display board. J121 is located at the rightrear corner of the board, under the ribbon cable disconnected in part d.
- f. Disconnect P117 and P148 from J117 and J148. J117 and J148 are located on the Timebase/Display board, at the right-rear corner and center-rear edge, respectively.
- g. Remove the three mounting screws securing the Timebase/Display board to the Center chassis and Power Supply.

- h. Using a 7/32 inch nutdriver, rotate the two black plastic retaining latches counterclockwise 1/4 turn to unlock them. The two retaining latches are located near the left-front and left-rear corners of the Timebase/Display board.
- i. Grasp the left edge of the Timebase/Display board and rotate it (and the Top chassis) upward about 45 degrees. While supporting the Top chassis, disconnect the ribbon cable connector at J131 (left-front corner of the Timebase/Display board) and the flex cable at J125 (right-rear corner of the Processor board on the underside of the Top chassis).
- j. Continue to rotate the Top chassis until it is at a 90 degree angle to the top of the instrument.
- k. Rotate the black retaining latch (center-left edge of the Timebase/Display board) 1/4 turn counterclockwise to release the board from the Top chassis.
- I. Grasp the left edge of the board and pull it slightly away from the Top chassis until it clears the head of the retaining latch unlocked in part k. Pull up on the board until the right edge of the board slips out of the four channel notches on the Top chassis.

Reverse parts a through I to install the board to the Top chassis and to secure the Top chassis to the Center chassis. Take care to fit the right edge of the board to the four channel notches when installing the board on the Top chassis.

3. Processor Board Removal

- a. Perform Step 1 to remove the cabinet.
- b. Set the instrument on a flat, smooth surface, with its underside facing down and the Front panel facing forward.
- c. Remove the three mounting screws securing the Timebase/Display board to the Center chassis and Power Supply.
- d. Using a 7/32 inch nutdriver, rotate the two black retaining latches counterclockwise 1/4 turn to unlock them. The two retaining latches are located near the left-front and left-rear corners of the Timebase/Display board.

- e. Grasp the left edge of the Timebase/Display board and rotate it (and the Top chassis) upward about 45 degrees. While supporting the Top chassis, disconnect the ribbon cable connector at J131 (left-front corner of the Timebase/Display board) and the flex cable at J125 (right rear corner of the Processor board on the underside of the Top chassis).
- f. Continue to rotate the Top chassis until it is at a 180 degree angle to the top of the instrument. The top of the Processor board is now exposed.
- g. Disconnect the ribbon-cable connector from J103 and the flex cable connector from J207 of the Processor board. J103 and J207 are located at the left-front corner of the board.
- h. Disconnect the ribbon cable connector at J123 of the Processor board (instruments with Option 05 installed only). J123 is located at the rear quarter section of the board near the center.
- i. Disconnect the ribbon cable connectors at J181 and J120 of the Processor board, J181 and J120 are located at the left rear corner of the board.
- j. Rotate the black retaining latch (center-right edge of the Processor board) 1/4 turn counterclockwise to release the board from the Top chassis.
- k. Grasp the right edge of the board and pull it slightly away from the Top chassis until it clears the head of the retaining latch unlocked in part j. Pull up on the board until the left edge of the board slips out of the four channel notches on the Top chassis.

Reverse parts a through k to install the board on the Top chassis and to secure the Top chassis to the Center chassis. Take care to fit the edge of the board to the four channel notches when installing it on the Top chassis.

4. Front Panel Board Removal

- a. Perform Step 1 to remove the cabinet from the instrument.
- b. Set the instrument on a flat, smooth surface, with its underside facing down and the Front panel facing forward.

- c. Pull straight out on the INTENSITY control knob to remove it from its shaft.
- d. Using a small, flat-bladed screwdriver, gently pry loose and remove the top trim cover.
 - e. Remove the four screws exposed by part d.
- f. Turn the instrument over to expose the bottom of the trim ring and remove the two screws securing the front feet to the instrument. Remove the feet from the trim ring.
- g. Remove the two remaining screws securing the trim ring.
- h. Grasp the edges of the trim ring and pull forward to remove it from the Front casting.
 - i. Turn the instrument over so its top side is up.
- j. Remove the three mounting screws securing the Timebase/Display board to the Center chassis.
- k. Using a 7/32 inch nutdriver, rotate the two black retaining latches counterclockwise 1/4 turn to unlock them. The two retaining latches are located near the left-front and left-rear corners of the Timebase/Display board.
- I. Grasp the left edge of the Timebase/Display board and rotate it (and the Top chassis) upward about 45 degrees. While supporting the Top chassis, disconnect the flex cable at J125 (right-rear corner of the Processor board on the underside of the Top chassis).
- m. Continue to rotate the Top chassis until it is at a 180 degree angle to the top of the instrument.
- n. Disconnect the ribbon cable connector from J166 on the Low Voltage Power Supply board and push it towards the rear of the instrument. J166 is located at the left-front section of the board near the front corner of the Center chassis.
- o. Disconnect the ribbon cable connector from J150 at the front of the Side board.

- p. Remove the anode lead from its retainer and dress it away from the lower square hole in the Main chassis. Take care not to separate the male end of that lead from the female end.
- q. Disconnect the ribbon cable connector from J152 of the Main board. J152 is located in front of the High Voltage shield, at the lower left side of the instrument.
- r. Carefully route the connectors disconnected in parts o and q to the inside of the instrument.
- s. Gently push the backside of the Front Panel Control assembly until it is removed from the Front casting.
- t. To remove the Front Panel Control board from the Front panel, perform the following subparts:
 - (1) Using a 1/16 inch allen wrench, remove the CH 1 and CH 2 VOLTS/DIV control knobs, as well as the A and B SEC/DIV control knob.
 - (2) Pull straight out on the remaining five control knobs to remove them from their shafts.
 - (3) Turn the Front panel face down and remove the four mounting screws from the Front Panel Control board. Separate the Front panel from the board.

Reverse parts a through t to assemble the Front panel assembly and install it on the instrument. Take care to align the GPIB Status indicators to their holes in the trim ring when installing that band.

5. Main Board and Gain-Cell Board Removal

- a. Perform Step 1 to remove the cabinet from the instrument.
- b. Perform parts a through h of Step 4 to remove the Front Panel trim ring.
- c. Pull the Front Panel assembly forward until it is clear of the Front casting and the face of the Front casting is accessible (it is not necessary to disconnect the cables connecting the assembly to the main instrument).
- d. Remove the six screws securing the Main board to the Front casting. The screws are located on the face of the casting and are adjacent to the four BNC connectors.

- e. Disconnect the two flex cable connectors at J104 and J108, and the ribbon cable connector at J105, J104, J105, and J108 are located near the right-front corner of the board.
- f. Disconnect the three ribbon cable connectors from J111, J113 (TV Trigger option only); and J141 at the left edge of the board.
- g. Disconnect the cable connector from J107, located near the right-rear corner of the board, and from J106, located near center-front edge of the board.
- h. Remove the screw securing the end of the Power switch's extension shaft to the Front casting.
- i. Grasp the large extension shaft near where it joins to the small shaft of the power switch and pull it upwards from the Main board to disconnect it. Lift up and back (towards the rear of the instrument) to remove the extension shaft from the Front casting.

NOTE

When installing the extension shaft to the Power switch, push the small shaft to put the switch in the IN position. Insert the shaft into the Front casting, align the extension shaft to the small shaft, and push the button end of the switch until the two shafts are coupled.

- j. Using a 7/32 inch nutdriver, rotate the seven black retaining latches 1/4 turn counterclockwise to release them.
- k. Disconnect the flex cable connector from J114 and the two retaining latches. J114 is located in left-rear corner of the board.
- I. Remove the two mounting screws securing the Main board to Main chassis.
- m. Lift the board up from the instrument and back from the Front casting to complete the board removal.
- n. GAIN CELL BOARD REMOVAL: If one (or more) of the four Gain-Cell boards (mounted on right-rear corner of the Main board) is to be removed, turn the Main board over. Then desolder the 13 pins (two groups—one of five pins, the other of eight) that connect the Gain-Cell board to the main board, working from the bottom of the board. When the pins are free the board can be removed. To reinstall, remount and resolder.

Reverse parts a through m to install the Main board.

6. Side Board Removal

- a. Perform Step 1 to remove the cabinet from the instrument.
- b. Set the instrument on a flat, smooth surface with the Side board facing up and the Front panel facing forward.
- c. Disconnect the ribbon cable connectors from J111 and J141 of the Main board.
- d. Disconnect the ribbon cable connectors from J100 of the Timebase/Display board and J103 of the Processor board. The two connectors are attached to the same ribbon cable.
- e. Disconnect the ribbon cable connectors from J121 of the Timebase/Display board and J120 of the Processor board. The two connectors are attached to the same ribbon cable.
- f. Disconnect the ribbon cable connector from J150 of the Side board.
- g. Perform parts j through I of Step 4 to access the inside of the instrument.
- h. Disconnect the ribbon cable connector from J102 at the right front corner of the Low Voltage Power Supply board and route the cable to the outside of the instrument.
- i. Rotate the Top chassis back to the normal (installed) position. Using a 7/32 inch nutdriver, rotate the two retaining latches 1/4 turn clockwise to temporarily secure it to the instrument.
- j. Rotate the black retaining latch (near the front of the Side board) 1/4 turn counterclockwise to unlock it.
- k. Remove the mounting screw (center of the Side board) securing the Side board to the Main chassis.
- I. Lift the front of the Side board up until it clears the retaining latch and then pull the board forward, until it clears the channel notch at its rear edge, to complete the removal.

Reverse parts a through I to install the Side board in the instrument. Take care to fit the rear edge of the board to the channel notch when reinstalling to the chassis.

7. High Voltage Power Supply Board Removal

- a. Perform Step 1 to remove the cabinet from the instrument.
- b. Set the instrument on a flat, smooth surface with the High Voltage Supply board facing up and the Front panel facing forward.

WARNING

The CRT anode lead may retain a high-voltage charge after the instrument is powered off. To avoid electrical shock, ground the CRT anode lead to the metal chassis after disconnecting the plug. Reconnect and disconnect the anode-lead plug several times, grounding the anode lead to chassis ground each time it is disconnected to fully dissipate the charge.

- c. Remove the anode lead from the retaining hook that secures it to the Main chassis.
- d. Disconnect the CRT lead (male end) from the High Voltage Module lead.
- e. Remove the single screw securing the High Voltage Power Supply and lift the High Voltage shield off.

WARNING

The five mounting posts on the side of the High Voltage module (U565) may retain a high-voltage charge after the instrument is powered off. To avoid electrical shock, discharge these posts to the metal chassis through an appropriate shorting strap.

- f. Discharge the five posts on the side of the High Voltage module to the metal chassis.
- g. Disconnect the cable connectors from J172 and J173, located at the front edge of the board, and from J162 and J176, located the rear edge of the board.

- h. Disconnect the remaining ribbon connector from J105 on the Main board.
- i. Pry outward on either one of two retaining latches securing the fan on its mounting posts. As the latch clears the edge of the fan, pull the fan outward and away from the instrument to remove. The latches are located at opposite corners; one at the bottom corner nearest the rear, the other at the top corner nearest the front, of the instrument.
- j. Perform parts j through I of Step 4 to access the inside of the instrument.
- k. Disconnect the crt connector from the back of the crt.
- I. Rotate the two black retaining latches (near the front- and rear-left corners of the High Voltage Power Supply board) 1/4 turn counterclockwise to unlock them.
- m. While holding its nut (located between the crt shield and the adjacent Main chassis) stationary, remove the mounting post (near the center of the board) securing the High Voltage Power Supply board to the Main chassis.
- n. Lift the left edge of the board up to clear the retaining latches. Pull the board to the left, until its right edge clears the two channel notches, to complete the removal.

Reverse parts a through n to install the High Voltage Power Supply board. Take care to fit the left edge of the board to the channel notches when reinstalling the board.

8. Low Voltage Power Supply Assembly Removal

- a. Perform Step 1 to remove the cabinet from the instrument.
- b. Disconnect the ribbon cable connector at J113 of the Main board to access the mounting screw at the center of the Side board. Remove that screw.
- c. Remove the mounting screw at the center of the Side board. Note that for instruments with Option 05 installed, it is necessary to disconnect the ribbon cable connector at J113 of the Main board to access the mounting screw.

Maintenance—2440 Service

- d. Disconnect the ribbon cable connector at J148 of the Timebase/Display board.
- e. Perform parts j through I of Step 4 to access the inside of the instrument.
- f. Disconnect the ribbon cable connectors at J102 (right front corner of the Low Voltage Power Supply Supply board) and J166 (left front corner of the same board).
- g. Disconnect the flex cable connector from J207 at the left front corner of the Processor board.
- h. Remove the six screws and two extension posts securing the Low Voltage Power Supply cover (hereafter referred to as "the cover") to the Low Voltage Power Supply bracket.
- i. Remove the screw securing the cover to the Center chassis.
- j. Remove the two screws securing the cover to the Rear chassis. One screw is located immediately below the GPIB Connector, the other immediately below the PLOTTER X OUTPUT BNC.
- k. Lift the cover off the Low Voltage Power Supply bracket to remove.
- Disconnect the four cable connectors from P30, P60, P70, and P80 (located near the rear of the Low Voltage Power Supply board). Note the color coding of the cables to guide in reconnection of same.
- m. Using a 7/32 inch nutdriver, rotate the two black retaining latches (near the left and right front corners of the Low Voltage Power Supply board) 1/4 turn counterclockwise to unlock them. Repeat for the two latches located near the middle of the right and left edges of the board.
- n. Remove the mounting screw securing the Low Voltage Power Supply assembly to the Main chassis. The screw is located near the right-front corner of the board.
- o. Carefully route the disconnected cables away from the top side of the Low Voltage Power Supply assembly.

- p. Grasp the front of the Low Voltage Power Supply bracket and lift up until the Low Voltage Power Supply board is clear of the retaining latches unlocked in part m.
- q. Pull the board towards the front of the instrument (until its rear edge clears the two channel notches) while lifting upwards to complete the removal of the assembly.

Reverse parts a through q to assemble the Low Voltage Power Supply assembly and secure it to the instrument. Take care to fit the board to the channel notches when reinstalling the board.

9. Cathode Ray Tube Removal

WARNING

Use care when handling a crt. Breakage of the crt may cause high-velocity scattering of glass fragments (implosion). Protective clothing and safety glasses (preferably a full-face shield) should be worn. Avoid striking the crt on any object which may cause it to crack or implode. When storing a crt, place it in a protective carton of set it face down on a smooth surface in a protected location. When stored face down, it should be placed on a soft, nonabrasive surface to prevent the crt face plate from being scratched.

- a. Perform Step 1 to remove the cabinet from the instrument.
- b. Perform parts c through i of Step 4 to remove the trim band from the instrument.
 - c. Remove the implosion shield from the crt faceplate.

WARNING

The crt anode lead may retain a high-voltage charge after the instrument is powered off. To avoid electrical shock, ground the crt anode lead to the metal chassis after disconnecting the plug. Reconnect and disconnect the anode-load plug several times, grounding the anode lead to chassis ground each time it is disconnected to fully dissipate the charge.

d. Remove the anode lead from the retaining hook that secures it to the Main chassis.

- e. Disconnect the crt anode lead (male end) from the high-voltage module lead. Discharge the crt anode lead by grounding its tip to the metal chassis.
- f. Disconnect the cable from J172 at the right-front corner of the High Voltage Power Supply board.
- g. Perform parts j through I of Step 4 to access the inside of the instrument.
- h. Disconnect the crt connector from the back of the crt.
- i. Disconnect the single cable from the crt (accessed through a hole in the top of the crt shield).

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- j. Disconnect the ribbon cable at J148 of the Timebase/Display board.
 - k. Disconnect the flex cable at J104 of the Main board.

- I. Remove the eight screws (two at each corner) securing the crt frame to the Front casting.
- m. Remove the crt frame from the Front casting. Guide the flex cable disconnected in part k through its slot in the Front casting while removing the crt frame.
- n. Grasp the face of the crt and pull it forward, while guiding the crt anode lead and the other cable (disconnected in part f) through their holes in the crt shield. It may be necessary to reposition the ribbon cable (disconnected in part j) as the removal of the crt is completed.

Reverse parts a through n to install the crt. When installing the crt frame (removed in part m) to the casting, refer to Figure 6-3 for the method of installation.

10. Menu Switch Removal

- a. Perform Step 1 to remove the cabinet from the instrument.
 - b. Disconnect the flex cable at J104 of the Main board.

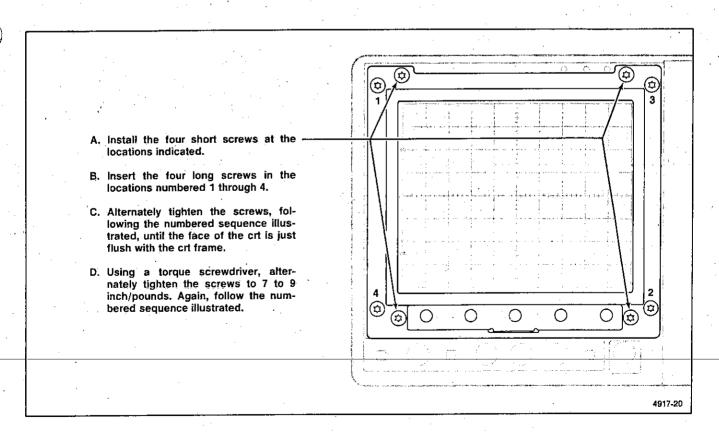


Figure 6-3. Installation sequence for installing the crt frame screws.

Maintenance—2440 Service

- c. Perform parts c through i of Step 4 to remove the trim band from the instrument.
- d. Perform parts k through m of Step 9 to remove the crt frame from the instrument.
- e. Carefully pull the adhesive-backed switch from the front of the crt frame.
- f. Pull the switch through the hole in the crt frame to complete the removal.

Reverse parts a through e to install the Menu switch to the crt frame and the frame to the instrument. Use care to align the switch to the locating studs on the crt frame when pressing the switch back on the frame.

11. Scale Illumination Board Removal

- a. Perform parts a through e of Step 10.
- b. Disconnect the Scale Illumination board cable from J106 (located near the front edge of the Main board).
- c. Remove the Scale Illumination board and the attached light reflector while guiding the cable (disconnected in part b) through its hole in the Front casting.
- d. Separate the Scale Illumination board from the light reflector to complete the disassembly.

Reverse parts a through d to install the Scale Illumination board to the instrument.

12. Attenuator Removal Procedure

- a. Perform Step 1 to remove the cabinet from the instrument.
- b. Perform parts b through s of Step 4 to access the inside of the instrument. Skip parts n, p, and q. When performing part r of Step 4, route the cable disconnected in part o.

- c. Insert the tip of a short screwdriver through the large slot in the front casting (above and right of the associated input BNC connector). Remove the screw securing the front of the Attenuator to the Main board.
- d. Insert the tip of a screwdriver through the hole in the Low Voltage Power Supply board that is directly above the Attenuator to be removed. Remove the screw securing the rear of the Attenuator to the Main Board.
- e. Rotate the Timebase/Display board to its mounting position and temporarily secure it by rotating the two black retaining lugs 1/2 turn clockwise to lock them. The two retaining latches are located near the left-front and left-rear corners of the Timebase/Display board.
- f. Remove the two screws securing the rear Attenuator shield to the heatsink. Remove the small shield.
- g. Unsolder the two Attenuator output leads from the variable-capacitor lead and the resistor-capacitor pair lead exposed in part f.
- h. Unplug the multipin connector from the Main board (at P147 for the CH 1 and P146 for the CH 2 Attenuator).
- i. Remove the two screws (one is immediately lower left and the other upper right of the associated input BNC connector) securing the Attenuators to the front casting.
- j. Remove the two screws securing the small bar to the bottom of the front casting.
- k. Grasp the front end of the Attenuator assembly by its BNC connector and the rear end by the rear edge of the Attenuator shield.
- I. Gently lift the Attenuator straight up from the Main board until the Attenuator pins clear their Main board plugs underneath the Attenuator assembly. Lift the rear of the Attenuator assembly up and towards the rear of the instrument until the Attenuator clears the braided shield cable mounted in the front casting.

Reverse parts b through I to reinstall the Attenuator. When performing part b, reverse parts b through s of Step 4 to reinstall the front panel and secure the Timebase/Display board and Front Panel assembly to the instrument.

DIAGNOSTICS AND INTERNAL CALIBRATION ROUTINES

INTRODUCTION

This subsection describes function and operation of the internal diagnostics and calibration routines. Where calibration routines make use of internal diagnostics, the interaction is explained. Status and other messages resulting from running the diagnostics or calibration routines are also detailed, and special conditions, such as the impact of power loss while certain diagnostic or calibration routines are running, are discussed.

In addition to the diagnostics and calibration routines, the Special Diagnostic menu and the features it accesses are also covered, including how they relate to the internal diagnostic routines. Information on how to run the diagnostics from the GPIB interface is included, followed by a table of Diagnostic/Troubleshooting procedures for this instrument.

OVERVIEW

This instrument supports two types of internal diagnostic tests and calibration routines. Self Calibration (SELF CAL) and Extended Calibration (EXT CAL) calibrate the analog subsystems of the scope to meet specified performance requirements. Any detected faults in the control system and/or in the self-calibrating hardware result in a "FAIL" message that labels the failed calibration type (SELF or EXT). Both SELF and EXT CAL make use of some of the diagnostic routines that comprise the Extended Diagnostics.

Self Diagnostics (SELF DIAG) and Extended Diagnostics (EXT DIAG) are the two types of diagnostic routines used to detect and isolate system operation faults in this instrument. The tests are based on a multi-level scheme. First the highest system level, the kernel, is tested, and then lower-level subsystems are progressively tested. Each lower-level subsystem tested follows a higher-level system that tested good. When the SELF DIAG detect a system fault, they isolate the fault-to-one of-the-upper-level subsystems immediately above the kernel. EXT DIAG can then be used to isolate the failure to lower-level subsystems and to test those subsystems, down to the lowest possible level.

In addition to the calibration and diagnostic routines just mentioned, there are the "Special" diagnostic features, useful for instrument troubleshooting, and Service Routines which are usually used with the Extended Diagnostics to isolate instrument failures.

CALIBRATION ROUTINES

SELF CAL

When the system runs the Self-Calibration routine, it generates test voltages to the Peak Detectors via the Cal Amplifier and DAC system. These voltage are used to set the gains, offsets and/or centering, and balance of the CCD Samplers, Peak Detectors, and Preamplifiers. The system uses iterative calculations to modify these voltages until converged solutions are reached; these converged solutions become the calibration constants stored in NVRAM (nonvolatile RAM) and are used to maintain calibration.

When SELF CAL is run, there is some interaction between the calibration routines for the different analog circuits calibrated. This interaction is minimized by using calibration constants obtained from the last SELF CAL run as starting values for calculating the new calibration constants when a new SELF CAL is run. If you are running a SELF CAL after a "COLD START" (see "SPECIAL Routines" in this section), the previous calibration constants are discarded; therefore, the SELF CAL tests are done twice to assure a converged solution. (The time required to perform the SELF CAL procedure from a COLD START is, therefore, obviously longer than the normal SELF CAL.)

SELF CAL can be run from the front panel using the EXTENDED FUNCTIONS menu or by the GPIB routines for automatically calibrating the internal analog systems. SELF CAL routines take about 10 seconds and calibrate most of the analog system. A SELF CAL may be performed by the user at any time (scope should be warmed up). Recommended times are when the ambient operating temperature changes by a significant amount since the last SELF CAL was run (see Level 7000-9000 Tests under "Diagnostic Test and Calibration Failures") and before a measurement is made which requires the highest possible level of accuracy.

EXT CAL

Extended Calibration is an interactive procedure requiring a Calibration Generator that produces accurate dc voltages and a fast-rise pulse. The dc voltages are used to verify the internal 10-V Calibration Reference and to adjust the gain of the Vertical system Preamplifiers and the gain and offset of the Trigger circuitry. The fast-rise pulse is used to determine a calibration constant that nulls the delay between channels.

The ADJUSTS routines generate test waveforms or voltage levels to be used in setting the gains for the CCD output amplifiers and the vertical and horizontal gain and offset for the CRT drive signal. Additional adjustments optimize the CRT display, including edge focus, geometry, CRT bias, etc. Since no two CRTs are exactly alike, these tests must be user-interactive.

The REPETitive calibration sets the slope of two internal timing ramps in the feedback system that locates points of repetitively-acquired data. REPETitive calibration is a *coarse* adjustment and should only be run after a COLD START. During instrument operation, a continuous *fine* adjustment maintains the calibration.

Other manual adjustments are: the CCD clocks; the CH 1 and CH 2 input capacitance; the 100-MHz bandwidth limit; the transient response; and (when the Video Option is installed) the 20-MHz bandwidth limit.

Extended Calibration via the GPIB makes it possible to calibrate any individual subsystem listed in the 7000-9000 levels of the Extended Diagnostics menu. This list includes all the subsystems normally calibrated collectively during during SELF CAL, as well as those adjusted in the various EXT CAL procedures when they are accessed from the front panel.

Calibration Operation

The steps and equipment needed to completely calibrate this instrument are found in Section 5, "Adjustments Procedure". Further information is found at the beginning of this section under "Instrument Calibration".

CAL/DIAG menu. All calibration routines are accessed by selecting CAL/DIAG from the EXTENDED FUNCTION menu (they can also be run via the GPIB). The EXTENDED FUNCTIONS menu is selected by the MENU/EXTENDED FUNCTIONS button when no other menus are displayed. Pressing the bezel button under the CAL/DIAG menu label produces the following menu display:

<status> <status> <warm-up-msg>
SELF EXT SELF EXT
CAL CAL DIAG DIAG

Pushing SELF CAL runs the previously described routine that calibrates this scope's analog subsystems. If the SELF CAL is successful, the PASS status is displayed above the SELF CAL button label in the CAL/DIAG menu. Failing SELF CAL causes the scope to enter the EXT DIAG menu (see Figure 6-5). If the CAL/DIAG menu is recalled, the FAIL status is displayed.

Pushing EXT CAL displays the EXT CAL menu:

<status> <status> <status> CTE
ATTEN TRIGGER REPET CAL ADJUSTS

Selecting ATTEN produces yet another menu:

<status> <status>
ATTEN CHAN
GAIN DLY

Pushing ATTEN GAIN, CHAN DLY, TRIGGER, REPET, CTE CAL, or ADJUSTS begins execution of the corresponding semi-automatic calibration routine. Completion of the ATTEN GAIN and TRIGGER calibrations requires the input of correct dc voltages, while the CHAN DLY and CTE calibration requires a fast-rise pulse.

EXT CAL routines can be aborted at any time by pressing the MENU OFF/EXTENDED FUNCTIONS button, but once a calibration routine (except ADJUSTS) has been started, it must be successfully completed or the status will be FAIL.

NOTE

Extended Calibration is considered a service function; therefore, the EXT CAL menus are normally disabled to make them unusable by the scope operator. The cabinet must be removed and Jumper J156 must be removed (diagram 13) to enable the menus. Disabling is done to prevent accidental loss of calibration by scope operators.

The <STATUS> message above the CAL labels indicates the results of the last test run for the calibration type above which it appears in the CAL/DIAG menu. When

a failure occurs, <STATUS> is *not* immediately updated; rather, a new test must be run to determine current status:

- a. During SELF CAL, some tests under levels 7000-9000 of the Extended Diagnostics are run. If any of these sublevel tests fails, the scope enters the EXT DIAG menu and indicates the level failed. Furthermore, the status label for SELF CAL in the CAL/DIAG menu is updated.
- b. For internal component failures that would cause EXT CAL to fail, the status is updated when EXT CAL is run, either from the front panel or GPIB, or upon instrument power on.

For calibration, <status> can be:

UNCALD:

Instrument has not been calibrated.

FAIL:

Hardware errors were detected during

calibration (calibration may not be valid).

PASS:

The instrument was successfully calibrated.

<warm-up-msg>. The actual message displayed is the warning "NOT WARMED UP". This message is displayed for approximately ten minutes after power-on to warn that calibration of the instrument during this period is not recommended.

The "NOT WARMED UP" message is displayed after every power-on, even if the scope is turned off and then right back on. In this case, calibration may be performed one minute after completion of the power-on routine.

NOTE

Running an EXT CAL for ATTEN and/or TRIG calibration without inputting the correct DC voltage levels causes the "FAIL" message to appear above the ATTEN and/or TRIG menu labels but does NOT change the ATTEN and/or TRIGGER calibration. See the LEVEL 7000-9000 test information under "Diagnostic Test and Calibration Failures" for the test levels that run when EXT CAL is executed.

DIAGNOSTIC ROUTINES

The two main types of internal diagnostic routines are Self Diagnostics (SELF DIAG) and Extended Diagnostics

(EXT DIAG). Both types can be executed from scope menus. The Self Diagnostics, as well as those subtests below the 7000-9000 level that run when EXT CAL is executed, are a subset of the Extended Diagnostics.

EXT DIAG

The Extended Diagnostics include all of the automatic test routines internal to the scope. Although the EXT DIAG are run when SELF DIAG runs, the individual tests can be performed at several levels from the EXT DIAG menu and its submenus (see "Operation" below).

EXT DIAG. The Extended Diagnostics are set up in a multi-level structure, the hierarchy of which is:

0000

Top Level of the Extended Diagnostics. When run, the Self Diagnostics are done (see "Self Diagnostics" in this section).

1000-9000

Second level (first level under top level). When any of these nine levels run, all sublevel tests below the running second level are done. All eight of these second level tests (and their sublevel tests) run when level 0000 is executed (executing level 0000 runs the Self Diagnostics).

x100-x900

Third Level, where x is the most significant digit of the second level test the third level is under. When run, any sublevel tests are also run.

xv10-xv90

Fourth Level, where x indicates the second level and y the third level test the fourth level is under.

CAPABILITY OF EXT DIAG. The hierarchical structure just detailed allows selective testing and fault isolation/location of instrument subsystems from the highest to the lowest levels. The second levels are those subsystems immediately below the kernel and levels three and four are progressively lower subsystems of those sub-kernel systems. Status (FAIL, PASS, or blank for not tested) appears at the top and second levels in the EXT DIAG menu if Self-Diagnostics are run; lower levels must be selected and run to determine individual status of lower subsystems.

Maintenance-2440 Service

Any individual test selected can be made to loop to isolate signal path problems with external test and measurement equipment, once the area of failure has been determined by the automatic tests.

Any of the Extended Diagnostics tests may be accessed either individually or in selected groups using the EXT DIAG control menu. The tests use internal feedback and the digitizing capabilities of the instrument to minimize the need for applying external signals or for using external test equipment to troubleshoot. Testing of a failed area down to the lowest functional level possible (in some cases to the failed component) provides direction for further troubleshooting with service routines and/or conventional methods. Troubleshooting a failure may be based on assumptions made possible by running selected tests to verify good circuit blocks, thereby eliminating those blocks from consideration as a failed area.

SECOND LEVEL TEST DESCRIPTIONS. When the second-level (1000-9000) test is run, the following systems are tested:

Test 1000	System ROM is checked to validate memory operation.
Test 2000	Read/Write and Addressing tests are performed on registers.
Test 3000	System RAM is checked for write-read capability to all addresses.
Test 4000	Front panel processor is checked
Test 5000	Waveform processor is checked.
Test 6000	Checksums of NVRAMS are done to validate the stored calibration constants and waveform data.
Test 7000-9000	Calibrated analog circuits are tested to see if they will pass

It is important to realize that, although status of the tests is indicated at the sublevels immediately below the kernel (1000, 2000, etc.), the tests are also run at any lower levels (3rd, 4th, etc.) in order to check out the indicated circuits. The only exceptions are as follows:

constants.

with the present calibration

- Levels 3700 and 3800 may only be executed from EXT DIAG and then only if internal jumper J156 is removed.
- CKSUM-NVRAM tests at level 6000 are only executed at power-on. When selected from EXT DIAG, only the flag status is changed.
- 3. The ATTENUATOR test at the 8700 level, the EXT TRIG OFFSET and GAIN tests (9114-17, 9124-27, 9213-16, 9223-26), and the REPET test (9300) are not run when Self Diagnostics are run. Neither are these tests run from the EXT DIAG menu. These tests are run when EXT CAL is run for ATTEN, TRIG, and/or REPET respectively.

SELF DIAG

The Self-Diagnostic routine runs the 1000-9000 level tests from the Extended Diagnostics. As mentioned, these diagnostic routines test the function of all subsystems immediately below the kernel level (the kernel being the "highest" level) and the lower-level systems below each subsystem. The tests of subsystems immediately below the kernel are shown as levels 1000-9000 when the EXT DIAG menu is displayed (see Figure 6-5). See the descriptions under "Second-Level Tests" for details on the circuits tested.

BINARY CODE FOR FAILED TESTS. In most cases, the EXT DIAG menu is the major tool in determining causes of internal failures. In the case of a failure that keeps the scope from displaying its EXT DIAG menu, the TRIGGER LEDs flash a binary code that indicates the FIRST test that failed:

As Self-Diagnostic tests run, the Trigger LEDs flash indicating that the self tests are being run. In a normal sequence with no failures, the tests run quickly, and the length of time that an LED is lighted is short. If a failure occurs, the Trigger LEDs flash a binary code of the FIRST failed test (see Figure 6-4 for the binary codes of the LEDs). This failure display is important, since it can be the only troubleshooting clue available if the scope cannot display the extended diagnostics menu.

For example, if test 2130 should fail, the following sequence of LED flashes occur to indicate the failed test number:

1. All the LEDs are lit at the start of Self Diagnostic routine to verify they can be turned on.

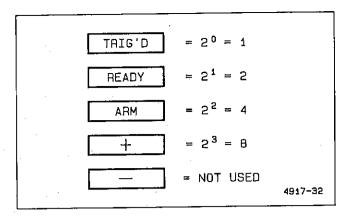


Figure 6-4. Trigger LED binary coding for diagnostic tests.

- 2. The LED's flash, indicating that tests are being run.
- When the test failure occurs, all the Trigger LEDs are lighted and held on momentarily, indicating a failure has been found.
- 4. For the first number of the failed test, the READY LED turns on for a binary 2 (the failed test is in the 2000 level); all the LEDs are then turned on to delimit the first digit of the failed test from the second digit to follow.
- 5. The second number of the test number (one) is shown by turning on the TRIG'D LED for the binary code for 1, then all the LEDs are again turned on as the code digit delimiter.
- 6. The third number of the failed test (three) is shown by turning on both the TRIG'D and the READY LEDs. Their binary values are summed (1+2) to obtain the third number of the failed test (three), and all the LEDs are again lit to separate the digits.
- 7. The fourth and final number of the failed test is 0, and all the LEDs light to identify the end of the failed test code.
- 8. After flashing out the coded number of the first failed test, the diagnostics continue on with the remaining tests, if they can be run. Any additional failures found will NOT be flashed on the Trigger LEDs.

If you miss the code the first time (as is usual unless you are expecting a failure), Self Diagnostics must be run

again. If a failure prevents display of the EXT DIAG menu, you must turn off the scope and turn it back on again to rerun the tests. It takes a little practice to read the failure codes from the LEDs.

If it can, the scope displays the Extended Diagnostics menu if a failure is found (or if the Self Diagnostics were run from that menu). The display of test selections in the Extended Diagnostics menu is a hierarchically structured set of tests in lists containing the test numbers, test names, and last status of the test results. If the test has not been run since the last COLD START, no status will be displayed. If an upper level test in the set (such as REG) is run, all tests in the REG test hierarchy will be done and labeled with a PASS or FAIL status. Menu operation is covered in "Diagnostics Operation".

Diagnostics Operation

Diagnostics are runnable from the front-panel or via the GPIB. The Self-Diagnostics are also executed when the instrument is powered up. For both the Self and Extended Diagnostics, front-panel access is from the same CAL/DIAG menu used to access the calibration features:

<status></status>	<status></status>	<status></status>	<warm-up></warm-up>
SELF	EXT	SELF -	EXT
CAL	CAL	DIAG	DIAG

Pushing SELF DIAG or powering up the scope causes the Self Diagnostics to run. These routines take about 30 seconds. First the TRIGGER status LED's flash as previously described. Then, if all tests are passed, the scope displays the main EXT DIAG menu if SELF DIAG was run from that menu, or returns to scope mode at power-down if SELF DIAG was run due to power-on. If passed when run from the CAL/DIAG menu, the scope returns to that menu and indicates the PASS status above the SELF DIAG button label. Failure of a test always returns the EXT DIAG menu regardless of what caused the SELF DIAG to run. The EXT DIAG menu is exited by pressing OFF/EXTENDED FUNCTIONS front-MENU panel button.

DIAGNOSTIC MENUS. Since the diagnostics routines are layered into a multi-level, hierarchical structure, the diagnostic menus are also layered this way. In each menu, there is one higher level test displayed, along with several equal sublevels. The menus are used to either run the higher (top) level test or to select a menu for one of the sublevels displayed. The select sublevel test can then be run as the top level of the submenu selected. Examination of the EXT DIAG menu should illustrate the structure:

Pushing EXT DIAG displays the main Extend Diagnostics menu (see Figure 6-5). In this menu, the top level test is listed as "EXTENDED DIAGNOSTICS" and its level number is "0000". The status at the time the test was last run is also indicated on the display line. All the other tests listed are one level below this level (1000-9000) and are indented to indicate their subordinance. The bottom three lines appear in this main menu and all submenus for use in selecting and running tests.

UP/DOWN ARROWS. The up-arrow and down-arrow buttons move an underscore pointer through the displayed list of diagnostic tests. Moving the pointer to a diagnostic below the top-level test line and then pressing the RUN/SEL button selects a submenu of tests available at the next level down with that diagnostic. Moving the pointer up above the top-level test line returns to the next level of hierarchy in the menu (if not in the main diagnostic menu; at the top—test 0000)—of the main menu, pressing the up-arrow button returns the CAL/DIAG menu).

A press of RUN/SEL with the pointer at the top line (top level) causes all the tests at and below that diagnostic level to be run. An individual test can be selected by using the arrow keys to move the pointer to the desired test, then pressing the RUN/SEL button twice (once to select it, and once to run it). The cumulative result of any test run will be displayed on test completion at the right of the title line. This will be either PASS, FAIL, or blank if an attempt was made to run a non-automatic test.

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Figure 6-5. Main EXT DIAG Menu.

NOTE

A diagnostics name in the Extended Diagnostics menu followed by an asterisk is not testable. The asterisk indicates either that the test is run only during an EXT CAL or run at power-on SELF DIAG only. The PASS/FAIL status is the result of the last EXT CAL or the last power-on check. A FAIL label on an asterisked test is accompanied by the "RUN SELF CAL THEN RUN EXT CAL" diagnostic message above the bezel button labels. An UNCALD label also appears above the uncalibrated selection of the EXT CAL selection in the CAL DIAG menu.

MODE. The MODE button rolls through four mode choices for running the selected test. The choices are RUN ONCE, RUN CONTINUOUS, RUN UNTIL FAIL, and RUN UNTIL PASS. If RUN CONTINUOUS is chosen before starting the selected test, it will be continually executed until the HALT button is pressed.

NOTE

If one of the continuous MODEs is chosen, pressing the HALT button will stop the test as soon as it completes AS LONG AS THE HALT LABEL IS SOLIDLY DISPLAYED above the button. If level 4000 is run, the display will be flashing and the HALT button is ignored (instrument must be powered down, and then up, to stop execution).

RUN UNTIL PASS and RUN UNTIL FAIL modes may also be stopped using the HALT button. In addition, all tests (except a looping Front-Panel μ P test) can be aborted with the MENU OFF/EXTENDED FUNCTIONS button. If an asterisked test (not presently testable) is selected, the mode switches to RUN ONCE and RUN ONCE, and the test does not run.

HALT—Pressing HALT causes all diagnostic test activity to stop at the finish of the current test in progress. It is especially used to halt a test running in a continuous mode.

Remember that, when using any Extended Diagnostic menus, the top (default) level test in the menu is the only one that can be run from the menu displayed. For example, moving the pointer to underline "3000 SYS RAM" in the main menu and pressing RUN/SEL selects (displays) the System RAM submenu with 3000 SYS RAM underlined and at the top level. Pressing RUN/SEL runs the 3000 level test. Moving to, say, "3500 A11U440" (a sub-

level in the displayed menu) and pressing RUN/SEL selects another lower-level submenu where the 3500 level test is the top level. This process can be continued until the lowest levels are reached.

STATUS. The status for the test at the time the last test is run appears next to the test names. For diagnostics <status> can be:

(blank)

test has not been executed.

FAIL

test failed on last attempt.

test passed on last attempt.

PASS

The <status> appearing on the test lines requires some interpretation. If <status> is for the top-level test (see above) for ANY EXT DIAG menu, PASS means ALL the sublevel tests THAT RUN when the top level is run passed; FAIL means at least ONE of the sublevel tests THAT RUN failed. If the operator has entered an EXT DIAG menu and not yet run the top level test, the status is

For any sublevel test displayed below the top level in a menu, STATUS is FAIL if any test in the submenus below that test was failed the last time it was run, whether or not it normally runs when the test in question runs (it is PASS if all are passed). In the case of a failed EXT CAL test, the upper-level tests which the failed test ran under will have FAIL status in the menus in which they appear as sublevel tests.

To illustrate the difference in interpretation just described, if the ATTENUATOR test, level 8700, failed at the last time the EXT CAL was run, SELF DIAG (level 0000) will pass if run because SELF and EXT DIAG do not run EXT CAL tests. However, level 8000 in the EXT DIAG menu will have FAIL status, since one of the submenus under level 8000 has FAIL status. If level 8000 is underlined and RUN/SEL used to select and then run the level 8000 test, it will pass, again because the 8700 EXT CAL test is not run.

To summarize, the top level status applies to all the tests that run under it, if the top level is run, or is blank if not run. Status on a sublevel test in menus applies to all tests in the submenus that fall under that sublevel test in the menu hierarchy, whether actually accessing and running the sublevel test would run those tests or not.

NOTE

The status for sublevel tests in the EXT DIAG menus can also be blank. Blank status indicates that the results of the tests below the sublevels is unknown, such as when a COLD START has been performed.

Diagnostic Test and Calibration Failures

Failures of the diagnostic tests run as a result of executing Extended or Self Diagnostics, as well as those run due to performance of SELF or EXT CAL, are now discussed. Some tests are run only under special circumstances (such as only as the result of running an Extended Calibration or when an internal jumper is removed). The circumstances are described as the individual levels are discussed.

LEVELS 1000-5000. Tests in the 1000-5000 levels are hardware tests that run when Self Diagnostics or Extended Diagnostics are run. If the instrument fails a 1000-5000 level test, the instrument displays the message "HARDWARE PROBLEM-SEE SERVICE MANUAL" in the Extended Diagnostics menu. The second level test that failed will be indicated by the FAIL status on the test line. This message remains displayed until POWER-ON Self Diagnostics pass. Running and passing the failed test, either from the Extended Diagnostic menu or via running Self-Diagnostics from the CAL/DIAG menu, does not remove the message. Hardware failures should be referred to qualified service personnel.

Test levels 3700 and 3800 test the RAM devices that store the internal calibration constants. Loss of power while these tests run can result in the loss of these constants. To prevent such loss, this instrument will only run those tests if an internal jumper, J156 (see Diagram 18), is removed before the tests are run. Run these tests only if necessary; this would normally be if a 6000 NVRAM failure has occurred and testing of device functionality is desired. In the event calibration constants are lost, SELF CAL and any calibrations labeled "FAIL" or "UNCAL" must be performed.

LEVEL 6000 Tests. The LEVEL 6000 diagnostics test the calibration constants, last front-panel setup, waveform, and Sequencer data stored in NVRAM. These tests are only run as Self Diagnostics at power on. Failure of a 6000 subset diagnostic test indicates a checksum failure of the stored data in the nonvolatile RAM. If test 6100 fails, tests 6200, 6300, and 6400 in the subset are not done.

Maintenance—2440 Service

The causes of a failure in the 6100-6300 bracket may be non-fatal to continued instrument operation, and normal (or near-normal) operation may be recovered by the user (also see "COLD START" under "SPECIAL Diagnostics" in this section):

a. LEVEL 6100. If the calibration constants are lost, this test will fail and the instrument will do a "Cold Start". The Extended Diagnostic menu will be entered and the message "RUN SELF CAL THEN RUN EXT CAL" will be displayed in that menu. Service personnel should perform the self calibration routine, plus the ATTEN, TRIGGER, and REPET Extended Calibrations. Unexplained loss of calibration constants indicates need for corrective maintenance.

b. LEVEL 6200. Loss of the stored power-off front-panel settings (failure of FP-LAST test 6200) causes the scope to do an INIT PANEL on power-up (see Table 6-7 for the INIT settings). Recovery of normal operation is done by pressing MENU OFF/EXTENDED FUNCTIONS to exit EXTENDED DIAGNOSTICS and resetting the front-panel controls to the required settings for the measurement to be made. The "FAIL" condition for test 6200 will be reset to PASS and the scope will not enter EXTENDED DIAGNOSTICS on the next power-up if permanent failure of the memory has not occurred.

c. LEVEL 6300-6400. Checksum failures of these levels indicate that waveform data and/or scaling information, or front-panel setups stored as sequences, are invalid. This may have occurred due to a memory failure or battery backup failure, or due to loss of power during the time the information was stored. Scope may be usable; recovery of operation is as for level 6200, above. The "FAIL" condition for test 6200 will be reset to PASS and the scope will not enter EXTENDED DIAGNOSTICS on the next power-up if permanent failure of the memory has not occurred.

LEVEL 7000-9000 Tests. Test failures at this level can be due to hardware or other causes:

a. A FAIL status (or PASS, for that matter) of the ATTENUATOR test (8700 level), the EXT TRIG OFFSET(9114-17 and 9124-27 levels) and/or GAIN tests (9213-16 and 9223-26 levels), and/or the REPET test (9300 level) are the result of the test(s) run at the time an Extended Calibration of the affected area(s) was last performed. These tests are not run when Self Diagnostics are run and are followed by an asterisk "*" after their test name to indicate this. (Neither can these tests be run from the EXT DIAG menu; however, since the FAIL status at the second level (8000 and/or 9000) might or might not be

the result of the sublevel Extended Calibration test, the EXT DIAG can be used to determine if it was an EXT CAL test that failed.)

Although these tests are not run at the Self-Diagnostic level, a failed status will result in the instrument displaying the Extended Diagnostics menu when the Self Diagnostics are run at power-on (Self-Diagnostics can PASS, however, since these tests are NOT actually run). The message "RUN SELF CAL THEN RUN EXT CAL" will be displayed in the menu. The message can only be removed by running the Extended Calibration for the failed test (either ATTEN, TRIG, or REPET). Extended Calibration is a service function and should be referred to qualified service personnel.

NOTE

In the case of an invalid standard voltage being applied during the ATTEN or TRIG Extended Calibrations, this instrument does not change its calibration and its accuracy is unchanged. The previously described conditions for a failed extended calibration are exhibited, however, and a valid Extended Calibration is required to remove the message from the Extended Calibration menu.

b. The remaining tests that run below the 7000-9000 level are executed when either a SELF CAL is performed or Self or Extended Diagnostics are run. (When run due to a SELF CAL, the system flags these appropriate tests as failed if a converging solution cannot be found; when run due to performing Self or Extended diagnostics, the system widens the limit values stored as calibration constants and tests if converging solutions could be found and a SELF CAL passed if it was run.) Failure of these tests causes the second level status to fail for the affected area and, if Self Diagnostics was run because of power on, the EXT DIAG menu is displayed indicating the failed status. The Extended Diagnostics can then be used to determine if the failed test is SELF CAL or EXT CAL related.

If the failure is not an EXT CAL related test(s), a hardware failure can still not be assumed unless SELF CAL is performed and a failure occurs in the same test or tests. Failure may only indicate that calibration is inaccurate for the current ambient temperature. This is because the tests are run somewhat differently when they are run as a result of running Self or Extended Diagnostics than when they are run as a result of running a SELF CAL, as was just mentioned.

When SELF CAL runs, the old values are modified and new values are calculated for the calibration constants; these new values are stored and then used to run the tests. One of the criteria for modifying these constants is ambient temperature.

When the tests are run due to SELF or EXT DIAGNOS-TICS, the old values are NOT modified. If the ambient temperature has changed sufficiently to affect calibration, the tests run may not be able to converge to the correct limits (even though they are wider than those of SELF CAL). This indicates that a SELF CAL should be done to move the calibration constant values to the new "in-calibration" limits to compensate for the present instrument conditions, whereupon the SELF DIAG test should pass. Failure to pass the SELF CAL procedure as outlined in Section 5 of this manual indicates a probable hardware failure and this instrument should be referred to qualified service personnel.

NOTE

If power is lost while SELF CAL is running, the calibration constants are invalidated. Normally, invalidating the constants causes the instrument to do a Cold Start to replace the invalidated constants with nominal values. If power interruption during SELF CAL causes the invalidation, however, the scope locks itself into the EXT DIAG menus and can only be exited by pressing the "up arrow" button. Pressing this button locks the scope into the CAL/DIAG menu, where the user must execute a SELF CAL before the menu can be exited. Running the SELF validates and preserves CAL calibration constants.

Special Diagnostics

The Special Diagnostic Features menu is accessed by pressing the menu button labeled SPECIAL in the EXTENDED FUNCTIONS. The features in this menu are normally disabled to prevent operators (non-service personnel) from operating them, and, if the SPECIAL menu button is pressed, the message "DISABLED—SEE MANUAL" is displayed. If J156 (located on the A13 board and shown in diagram 13) is removed, "WARNING: SERVICE ONLY—SEE MANUAL" is displayed in the SPECIAL menu and the menu is enabled to allow the features to be used for servicing the scope.

COLD START. COLD START eliminates all the previous calibration constants and restores them to known nominal values. A COLD START is especially useful for removing scrambled data from the NVRAM and is needed to permit a valid SELF CAL (and subsequent testing) to be performed if the data scrambled is the instrument's

calibration constants. After a COLD START, a SELF CAL and the ATTENuator, TRIGGER, and REPET EXT CAL must be performed to return the instrument to its previous state.

A COLD START can be initiated in three ways. One, J156 can be removed and the SPECIAL Diagnostics menu can be used to COLD START the scope as an aid in servicing it. Second, a COLD START is done upon power-up if the Lithium battery that backs up the System NVRAM is changed or fails, or if the NVRAM is relaced. Third, if the internal calibration constants are corrupted, the instrument fails test level 6100 and, the next time it's powered up and the Self Diagnostics are run, a COLD START is performed. (The only exception is when the instrument detects that an interruption of power during SELF CAL caused the constants to become corrupted—see NOTE under LEVEL 7000-9000 Tests failures earlier in this subsection.) The latter two COLD STARTS described here can occur whether J156 is installed or removed.

After a COLD START, the instrument displays the EXT DIAG menu, where the test level numbers, test names, and last status of the test results is displayed. If the test has not been run since the last "COLD START," no status will be displayed. If an upper level test in the set (such as REG) is run, all tests in the REG test hierarchy will be done and labeled with a PASS or FAIL status. Menu operation is covered in "Diagnostics Operation".

FORCE DAC. Pressing this menu button accesses a menu that lets service personnel vary selected adjustment constants to aid in troubleshooting certain internal circuits. It is especially useful for facilitating troubleshooting of the digital-to-analog converter circuitry and all the output sample-and-hold circuits of the DAC System. The routines in Table 6-6 indicate how this feature is used.

CAL PATH ON:OFF. When ON, the calibration signal path to the Peak Detectors is closed. If large offset errors have driven the display off-screen, switching CAL PATH ON eliminates the Attenuators and Preamplifiers from the input signal path and places the calibration reference level on the display. If that brings the display back on screen, the offset problem may be isolated to the Attenuators or Preamplifiers; if not, then the problem may be in the Peak Detectors or CCDs.

Service Routines

The Service Routines are menu, GPIB interface, or jumper initiated routines for exercising the hardware, usually in a looping mode, that allow a service person to

troubleshoot an internal fault using external testing and measuring equipment. Where possible, the Extended Diagnostics routines are used for looping to allow access to them from both the front-panel EXTENDED FUNCTIONS menu and the GPIB interface.

Jumper-initiated tests include Kernel Mode for the System μP and the Waveform μP , Waveform μP Bus Control Mode, Bus Isolate Mode, System μP Chip Select test, Resets for the System μP and the Waveform μP , a Front Panel μP internal diagnostics test, and a Front Panel Multiplexer test. A description of these tests and how they are used is included in Table 6-6, Extended Diagnostics.

Troubleshooting routines (written by a system programmer) that systematically exercise specific firmware or hardware functions can be implemented via the GPIB interface. This type of external testing provides a tool for troubleshooting the scope that may be changed as needed by controller programming.

Use of the Service Routines provide service personnel with signals and procedures that enable fault isolation and restoration of an instrument to a functional level that is supported by the Extended Diagnostics and/or other routines.

DIAGNOSTICS OPERATION VIA THE GPIB INTERFACE

Operation of the GPIB interface is described in the Programmers Reference Guide supplied with this instrument. This additional information describes use of the diagnostic commands. Operation of any of the four Cal/Diagnostic modes is selected by using the keywords SELFCal, EXTCal, SELFDiag, or EXTDiag as arguments with the TESTType command via a GPIB controller. The selected TESTType will start when the EXEcute command is received. See Appendix A of the Programmers Reference Guide for the definition of the GPIB calibration and diagnostics commands.

SELF CAL

If TESTType SELFCal is selected, the Self Calibration portion of the test sequence will run in its entirety when the EXEcute command is received. A service request (SRQ) will be issued when the sequence is finished if the OPC mask is on. The status byte received by the controller will indicate if the test completed either with error or with no error. See the Programmers Reference Guide for a list of the status bytes.

If an error occurs during SELFCal, it is reported to the controller when the ERRor? query is issued to the instrument. ERRor? returns a string of error numbers (up to nine) resulting from the last EXEcute command. These numbers will be the highest order in the hierarchy of the SELF CAL routine; so, to locate the exact test that failed in the tree, the TESTNum must be set to a lower level and the ERRor? query reissued until the lowest detection level of the failure is reached. The ERRor? query returns 0 if no errors have occurred. This method of failure location is used for errors generated by any of the calibration or diagnostics sequences.

EXT CAL

The EXTCAL TESTtype allows specifying the calibration sequence (TESTNum) to be performed. The calibration routine specified may be any steps or sub-steps of the EXT CAL or SELF CAL routines. The user is responsible for assuring that any externally required test equipment has been connected and programmed and that pauses in the procedure to make manual adjustments or equipment changes are terminated via a menu button push or a GPIB STEp command to advance to the next step in the sequence. The external calibration sequence numbers to be used as the numerical argument for TESTNum are listed in Table 6-6 under the "Test Number" column heading. The valid test numbers for Calibration are 7000 to 9300 in the table. Error handling is the same as in SELFCal.

SELF DIAG

Invoking the TESTType SELFDiag causes execution of the entire self-diagnostic sequence when an EXEcute command is received. Error handling is the same as in SELFCal.

When Self Diagnostics is called via the GPIB, completion and/or failure will cause an SRQ to be issued by the instrument. The status bytes returned on a poll indicate a successful completion or failure of the Self Diagnostics sequence. Errors can then be queried via the GPIB and traced to the lowest level of the Extended Diagnostics in the same manner as from the front panel. Failure of Self Diagnostics when run from the GPIB does not put the instrument into the Extended Diagnostics menu as it does when run from the front panel.

EXT DIAG

TESTType EXTDiag allows a specific TESTNum to be selected for execution upon receiving an EXEcute command. Error handling and reporting is the same as in SELFCal. Looping a test is done by issuing the LOOp command prior to the EXEcute command, and the HALt command stops the looping test.

DIAGNOSTIC PROCEDURES

The various tests resident in the scope are organized into a tree structure with a test number designating each node. The root node is 0000. A summary of the way in which the tests are performed and the type of test made follows the test number and test name in Table 6-6.

NOTE

FAIL and PASS flags in the Extended Diagnostics menu show the results of the last test run. If a defective device that has previously caused a FAIL flag to be set is replaced, the test must be run again to obtain a PASS indication in the menu.

These troubleshooting procedures are broken down into several types. The Troubleshooting Procedures of Table 6-6 provides a description of the tests made, and in many cases, the troubleshooting procedure used in case of a test failure. Other areas of the scope require more extensive troubleshooting trees. These areas are: the Low Voltage Power Supply, the Video Option, the Display System, and the Time Base and System Clocks. Troubleshooting trees are located in the "Diagrams" section of this manual. Some of the troubleshooting procedures are very general in that they don't lead the troubleshooter directly to a specific faulty component or components. In those cases, it is up to the troubleshooter to analyze the information obtained from the tests made to determine the actual fault. Figure 6-6 is a flow chart that shows the initial troubleshooting steps as an aid in determining where to start.

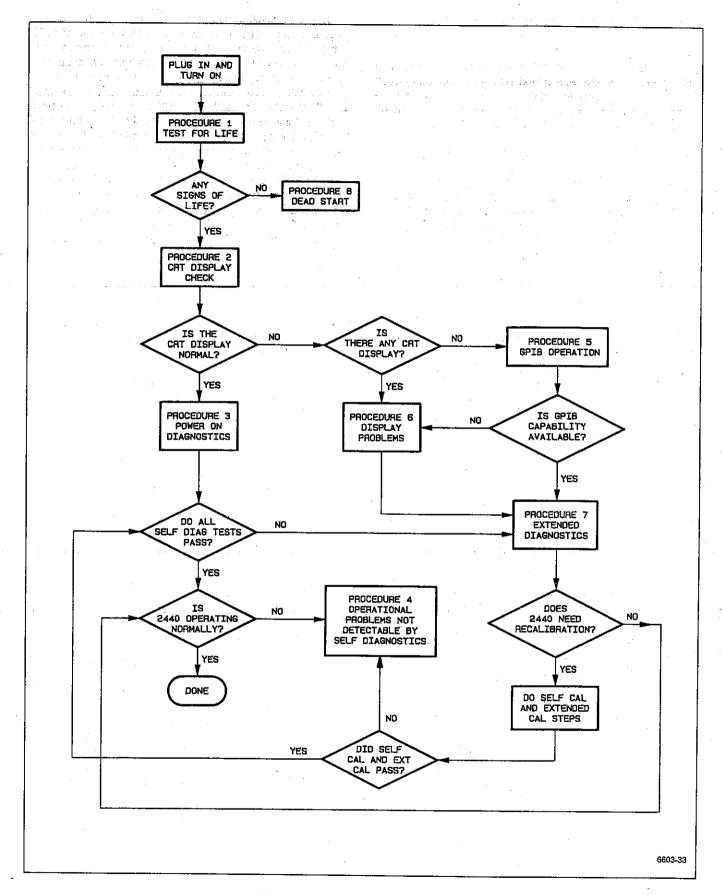


Figure 6-6. Initial troubleshooting chart.

Table 6-6 2440 Troubleshooting Procedures

1	INITIAL INDICATIONS
TESTS FOR LIFE	 Are TRIGGER LEDs flashing? If all lights are flashing, suspect Waveform μP ROM U480 or U490 (diagram 2) or their selects.
	 Is there activity from GPIB LEDs during turn-on? If the three LEDs above the crt (LOCK, SRQ, and ADDR) all light then go through a binary counting pattern (test number 2170), the diagnos- tics are working, and the instrument is alive. Go to Procedure 2.
•	3. After 30 seconds of turn-on, press MENU OFF and cycle the SLOPE switch. If the $+$ and $-$ Slope LEDs light alternately, the System μP is alive, and the operating system is active. Go to Procedure 2.
فهمت والأوادي والمدامية	4. Did the attenuator relays click? If the relays clicked, the power-on self tests vere running.
	5. If any of the signs-of-life occurred, then assume that there is some "life in the box" and go to Procedure 2; otherwise, go to Procedure 8.
2	CRT DISPLAY CHECK
· <u>. </u>	If the menus are normal (can focus, adjust intensity, etc.), then go to Procedure 3.
	2. If there are no displays then go to Procedure 5.
	 If there is a display, but the display is incorrect (no intensity control, out of focus, etc.), a dot only a vertical or horizontal streak, then it is an analog problem. Go to Procedure 6.
	4. If portions of the readout are missing or wrapped over, but the power-on test runs, the front-pane controls and the EXT DIAG menus may still be useful. Attempt to use the diagnostics to determine the failed tests. Also, read the binary code of the first failed test that is flashed by the Trigger LEDS during the power-on sequence. Use that information as a starting point for troubleshooting using the steps indicated for the failed test in Procedure 7, "EXTENDED DIAGNOSTICS". The most probable cause of a failure of this type is a bus problem or bad IC on a bus causing a stuck bit in Display circuitry of the Time Base/Display board (schematic diagrams 16 and 17). The busses to suspect are the ones connected to the IC indicated by the failed test.
3	POWER-ON DIAGNOSTICS
	NOTE: THIS IS NOT SELECTABLE, IT EXECUTES AT POWER-ON.
	1. If all the power-on tests pass, go to Procedure 4. If not, then go to Procedure 7.
4	OPERATIONAL PROBLEMS (Not detectable by diagnostics)
NO SIGNAL	Phase Clock Array Outputs A10U470 (schematic diagram 11)
ACQUISITIONS	1. Check A10U470 (Phase Clock Array) at pins 11, 12, 13, 14 and 15 for output clocks.
	2. If no outputs, the problem is probably U470 or the input circuit to U470 at pins 65 and 67; i.e., CR580 or C582.
	3. If the Phase Clock Array is working, the problem is in the Time Base.

TIMING ERROR AT 50 μs/div AND FASTER

Phase-Locked Loop Circuit (schematic diagram 11).

 Check the 10-MHz input to U381 pin 6. If there is no 10-MHz clock at TP174 then go to the Timebase troubleshooting chart (located in the "Diagrams" section) and troubleshoot the System Clocks.

NOTE

Use 2440 CURSOR function of 1/TIME to measure the frequency. The cursor position difference will read out directly in frequency.

2. Check U381 pin 9 for 10 MHz.

Frequency too low at pin 9:

a. Check that U381 pin 3 has negative pulses and that the voltage at U381 pin 12 is positive with respect to U381 pin 3. The VCO CTL voltage at TP581 can be as high as \pm 12 V.

Frequency too high at pin 9:

- b. Check that U381 pin 12 is ramping negative with respect to U381 pin 3 (average not absolute) and TP581 can be as negative as -0.6 V.
- c. If these conditions are not true, the problem is probably Phase/Frequency Detector U381 or amplifier U580.

MISSING DATA POINTS IN REPET

Jitter Correction Troubleshooting (schematic diagrams 12 and 13):

On the scope under test, select REPET acquisition mode, AUTO LEVEL, VERT trigger, DC Trigger COUPLING, and set the SEC/DIV setting to 5 ns. Then select ACQUIRE and connect a probe from the CH 1 input to TP291 (TTLB1) (found above A10U450, the CH 1 CCD, on the main board).

If there are bands of missing data points every two divisions, or only a few data points are placed every two divisions or the waveforms are distorted, the problem may be in the Jitter Correction circuitry.

The Jitter Correction circuit has both analog and digital circuits. First check the digital portion to insure that it is working. If that is ok, then assume that the problem is in the analog portion of the Jitter Correction circuit.

DIGITAL SECTION TROUBLESHOOTING

- Check that START1 and START2 are present at U841 pin 2 and U842 pin 2 (located on the Side board and shown on diagram 13) respectively and that they are coincident.
 - a. Test the collector of Q492 and Q391 (located on the Main board and shown on diagram 12) for the START pulses.

If missing:

- b. Check for SRAMP1 and SRAMP1 at the bases of Q492 and Q491.
- c. Check for SRAMP2 and SRAMP2 at the bases of Q391 and U390.
- d. Check for RAMP and RAMP at the bases of Q392 and Q490.

If any gating signals are absent, backtrack to U470 and/or U370 (on diagram 11) and locate the defective component.

- 2. Check that STOP1 and STOP2 are present at U841 pin 12 and U842 pin 12 (on the Side board). These signals are not coincident and should be littering with respect to one another. If missing, backtrack to U490 and/or U390 (located on the Main board and shown on diagram 12) to locate the defective component.
- While triggering on the START1 pulse, check for gated signal (by STOP1) at U852 pin 1 on the Side board. Check at U853 pin 1 for gated signal while triggering on the START2 pulse. If either gated signal is missing, check the gating components to locate the problem.
- While triggering on the START1 pulse, check for activity (fast to slow) at the Jitter Counter (U844 and U852) outputs (pins 14, 13, 11 and 12 on U844; pins 3, 4, 5, 6, 11, 10, 9, and 8 on U852). Observe that each output pin on the ICs should be switching slower than the preceding one as the counters count down. Replace the counter if found defective.
- Check that the inputs to U750 and U752 are gated to the outputs of U752. The only time they are the same is if both pin 1 and 19 are low. If a WORD trigger probe is not available, the following setup may be used making use of the A and B Trigger Mode to obtain coincident triggering.

HORIZONTAL

A and B SEC/DIV MODE

200 ns

В

VERTICAL

MODE

CH 1 and CH 2

COUPLING

DC

VOLTS/DIV

2 V

POSITION

Traces to graticule center

TRIGGER

A TRIGGER SOURCE

EXT1 A*B

A LEVEL

500 mV

SLOPE MODE

- (minus)

B TRIGGER SOURCE

NORMAL

EXT2

MODE

TRIG AFTER; EXT CLK OFF

Now connect the EXT1 to U750 and U752 pin 1 and EXT2 to U750 and U752 pin 19. The inputoutput pairs may now be checked, and they should compare at the "T" of the trigger point.

ANALOG SECTION TROUBLESHOOTING

- Connect a probe from CH 1 of the scope under test to the TTLB1 test point on its main board. Select REPET, set the scope under test to 2 ns/div and obtain a stable trigger.
- Set the test scope to 500 μ s/div.

With the test scope:

- Make sure that the signal at the collector of Q491 and Q390 stabilizes at about 800 mV. This is the baseline stabilization circuit. The waveforms shown next to the schematic diagrams are useful to make waveform comparisons.
- 4. Check for a fast ramp that corresponds to RAMP and RAMP from U370. This ramp should rise from the stabilization level to a maximum and start down at the same time that the START1 (or START2) pulse steps high, and that the STOP1 (or STOP2) pulse steps high when the descending ramp crosses 0 V. If not, troubleshoot the circuitry to determine the problem. These ramps should be linear both in rise and fall times.

GPIB -

GPIB Test for Activity (schematic diagram 20):

- Press the OUTPUT menu button, then SETUP, then MODE. Select L/ONLY and see if the ADDR LED is on. Select T/L and see if the ADDR LED is off. Select T/ONLY and see if the ADDR again is on.
- 2. If the LEDs follow the above, GPIB IC U630 is at least responding to the System μ P, and the problem is probably in GPIB Bus Buffers U720 or U624.
- If the LEDs do not follow the above pattern, troubleshoot bidirectional buffer U532 or U630 (assuming the LEDs do the 0 through 7 binary count during REG test section of EXT DIAG).

FRONT PANEL PROBLEMS

Front Panel and Auxiliary Front Panel (schematic diagrams 4 and 6):

If there is a front panel problem and the Extended Diagnostics have not detected anything, the problem is not in the Front Ranel Processor or its handshake logic with the System μP .

On the Front Panel μ P (U700), do the following checks:

NOTE

When probing around the Front Panel μ P circuitry, it is possible to cause bad data to be written to the System μ P and/or the Front Panel μ P by inadvertent grounding of pins or accidental shorting of pins together. If this should occur, many trouble symptoms may be present. To cure these symptoms, turn off the scope and turn it on again. This rewrites all RAM space in the System and Front Panel microprocessors with correct operating data.

- Check pins 26, 27, 28, 29, 30, and 15 for active output signal switching. These signals are all asynchronous, so a stable display pattern is not possible (without going to SAVE mode on the test scope).
- If the signals checked in Step 1 are active, go to Step 3. If these signals are not actively switching, perform the Front Panel MUXTEST to check that the μP drives the MUXSEL signal lines in a tight looping routine. In the MUXTEST, only the MUXSEL signal output lines are being driven. No output will be seen on the S/L or SHCLK lines (pins 29 and 30 respectively).
- Check pin 24 for active AOUT0 return signal from the Front Panel pots.
- 4. If the return signal line is active, go to Step 5. If it is not active, showing the different voltage levels from the Front Panel pots, troubleshoot Front Panel Pot Scanner U902 (an 8-to-1 multiplexer). Problems with a single pot output rather that a total failure of the Pot Scanner may be checked out using the MUXTEST mentioned in Step 2.
- 5. Check pin 25 for active return signal from the Front-Panel Switches.
- If the SW/OUT signal line is active, the Switch Scanner circuitry is working. If it is not active, troubleshoot 1-of-8 decoder U903 and serial shift register U904 for correct operation.
- 7. Check pin 22 (AOUT2) for an active return signal from the Auxiliary Front Panel INTENSITY pot and Front Panel BNC connectors. Individual signal voltage levels may be checked using the Front Panel MUXTEST if the signal line is active. If switching levels are not present on the AOUT2 signal line, troubleshoot 8-to-1 multiplexer U600.
- Check pin 9 (SWOUTA) for an active signal when one of the Auxiliary Front Panel buttons is pressed (bezel, SELECT, STATUS, MENU OFF). Otherwise, a HI is being shifted out of serial shift register U700. If the SWOUTA signal does not show a square pulse when one of the buttons is pressed, troubleshoot U700.

Front Panel MUXTEST:

An intermittent failure or noisy front panel pot can produce inconsistent control changes. To test individual pots for smooth operation and full range control limits, the Front Panel MUX SELECT test may be used to provide stable triggering.

- 1. Turn the power off and connect pins 2 and 3 of J155 together.
- 2. Ground the MUXINH signal at the end of R815 nearest the front of the 2440 to DGND.
- 3. Connect the test scope to observe the AOUT0 signal at R800 pin 8. Trigger the test scope on MUXSEL2 at R800 pin 4. Set the SEC/DIV switch to 100 μ s and the VOLTS/DIV to 2 V.
- 4. Power on the 2440. When it does the power-on test, it will signal a test failure of 4300 on the Trigger LEDs, and there will be no display on the 2440 crt.
- 5. Rotate the following rate position pots:

CH 1 Vertical Position CH 2 Vertical Position Horizontal Position Cursor/Delay Position

6. Check that the pots go into the rate region at both extremes of rotation and that the voltage level for each pot moves smoothly from one amplitude level to the other (approximately 0.5 V to 5 V total range) as the pot is rotated. See the test waveform illustration to identify the portion of the waveform associated with the control being rotated.

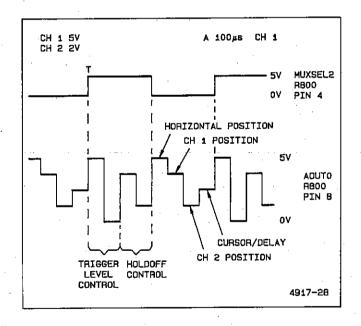


Figure 6-7. Mux Test waveforms.

7. Rotate the following infinite rotation pots:

Trigger Level Control Holdoff Control

- 8. Check that both sides of the pot have equal output range (approximately 0 V to 5 V) and that the voltage level for each side of each pot moves smoothly from one extreme to the other as the pot is rotated through the continuous range (not its end-switching region).
- Connect the test scope to observe the AOUT2 signal at R809. This signal is from the Auxiliary Front Panel circuitry.
- Momentarily short the shell of each of BNC input connectors to its coded-probe-switching ring and observe that the voltage level for that connector goes from 5 V to 0 V.
- 11. Rotate the infinite rotate INTENSITY pot and check for smooth voltage level changes on both sides of the pot (from approximately 0 V to 5 V).
- 12. The two remaining analog levels are the CH 1 and CH 2 50 ohm overloads. Check that they are approximately 3 V each.

BELL PROBLEM

Bell Circuit (schematic diagram 20):

Remove the word trigger probe, then:

 Connect a probe to the emitter of A12Q592. Then select the B TRIGGER SOURCE menu and press the BEZEL switch for WORD. The voltage should go close to +4 V with about a 1 V p-p, 2 kHz square wave superimposed upon it (peak of 5 V).

If the 4 Vdc is not present, check the signal path back to A12U760 pin 16. If the 2 kHz is missing, check back to the oscillator circuit A12U274.

CALIBRATOR PROBLEMS

Calibrator (schematic diagram 13):

NOTE

Make sure that you have not made the mistake of viewing the Calibrator signal output with a 10 M Ω probe and have the channel in 50 Ω input termination.

The calibrator circuit can be split into two parts. The source of the signal (CALCLK input at W122 pin 2) and the analog output stage on circuit board A13.

- 1. Check for a 3 V square-wave signal at the forward end of R831 (100 Ω resistor under A13U831 near the cable connector). If present, the problem is in U831, U731, Q831, or one of the parts in that output amplifier circuit.
 - a. Check U831 pin 8 for a signal.
 - b. Check U831 pin 2 for +2.4 V.
 - c. Check U831 pin 1 for +5.1 V.
 - d. Check emitter of Q831 is the same as the base of Q831.
- Check for a 3 V square wave at A11U680 pin 18. If present, the problem is a defective cable connection from A11 to A13 boards.
- Check for a square-wave signal at A11U680 pin 2. If present, replace A11U680.
- 4. Replace A11U670.

VIDEO OPTION

Video Option (schematic diagram 21):

If Video triggers are selected and the menu says not installed, then the diagnostics have detected a problem (if the option is installed). See Table 6-7, the Video Option troubleshooting table.

WORD TRIGGER

Word Trigger (schematic diagram 20):

- 1. Make sure the Word Trigger probe connector is properly installed (connector is on the 2440 rear panel).
- Select TRIG POSITION to 1/8, SEC/DIV to 100 μs, and VOLTS/DIV to 2 V. Probe A12U754 pin 5 for clock pulses. If not present, verify A12U754 pin 1 (RESET) is HI and A12U754 pin 11 has clock pulses. Replace A12U754 if the signals at pins 1 and 11 are ok.
- 3. Verify that the flex connector at the back of the A12 board is installed correctly. If ok, then the WORD RECOGNIZER probe is possibly defective. Try the probe on another 2440 to verify its operation.

DAC SYSTEM FAILURE

DAC System (schematic diagrams 5 and 6):

Symptoms are CCD and Peak Detectors gain fails SELF CAL, and Trig Level fails SELF CAL.

- 1. Check TP650 (found on the Main Board) for 0 V.
- 2. Check TP660 (also on the Main Board) for +1.25 V.
- 3. If the test point voltages are good, the DAC SYSTEM is operating normally to this point. Troubleshoot the DAC multiplexers (U831, U821, U960, and U830) and the individual DAC output ports (schematic diagrams 5 and 6).
- 4. If the levels at TP650 and TP660 are bad, check DAC multiplexer U651, the DAC inputs (U800 pins 1 through 12), and current-to-voltage converter U661C. Should see U661C having an output of 32 dc levels, switching from one to the next each 2 ms, and then repeating. The maximum output level is ±1.36 V. This output signal should be present at the input to each of the DAC multiplexers (pin 3), and each multiplexer output pin should have a steady dc voltage level present.
- 5. Check that only one DAC MUX enable at a time from U272 is LO.
- 6. Use the FORCE DAC test to check suspected output ports for correct control range.

Force DAC Test

1. Press the SPECIAL menu choice under Extended Functions and then press FORCE DAC.

NOTE

The SPECIAL menu choices are normally disabled to the user and press of the SPE-CIAL menu button calls up the display "DISABLED—SEE MANUAL". To enable the choices for servicing, the cabinet must be removed and Jumper A13J156 (EXT CAL DIS on diagram 13) must be removed.

- The first and second bezel buttons are used to select through the DAC values to be tested. The INTENSITY knob sets the values.
- 3. Test suspected DAC circuits for correct voltage limits over the control range using the test points and values given in the following Force DAC Ranges table.

Table 6-6 (cont)

Force DAC Ranges						
DAC	DAC FORCE DAC Values/		Voltag	e Range	Effect of	
Output	Output Location	DAC Voltage After Cold Start	0	4095	Increasing Value	
CH1Bal CH2Bal	U641-7 U641-1	2048/0.50	-1.37	1.36 V	Trace shifts down	
CH1Gain CH2Gain	U641-8 U641-14	1540/—4.37 V	-6.48 V	1.58 V	Gain decreases	
1POS	U630-1	2048/5 V ^a	-4.35 V	-5.66 V	Trace moves up	
GN11 GN12	U841-1 U841-7	2048/-0.50 V ^b	-1.37	+1.36	The channel and CCD side indicated by the DAC output is offset	
GN13 GN14 GN21	U841=8 U841-14 U951-1	The second of the second secon	and the second section of the sectio	ad Transfer on the long for the contract of the	from remaining sides.c	
GN22 GN23 GN24	U951-7 U951-8 U951-14					
CT11 CT12 CT13 CT14 CT21	U840-1 U840-7 U840-8 U840-14 U950-1	2048/—0.50 V ^d	+4.76	+12.1	The channel and CCD side indicated by the DAC output is offset from remaining sides. ^e	
CT22 CT23 CT24	U950-7 U950-8 U950-14					
CM10	U631-1⊷	1650/=0.27 V [†] 2000/—0.04 V 2200/—0.10 V	+4.76 +4.76 +4.76	+12.1 +12.1 +12.1	CH 1 CCD Sides 1 and 3 offset from 2 and 4.	
CM1E	U631-7	1650/—0.27 V 2000/—0.04 V 2200/—0.10 V	+4.76 +4.76 +4.76	+12.1 +12.1 +12.1	CH 1 CCD Sides 2 and 4 offset from 1 and 2.	

⁸DAC values for CH 1 and CH 2 POS are not written after a COLD START until an acquisition occurs; Turn off EXT DIAG menu and press ACQUIRE; then return to FORCE DAC.

bEach GNxx DAC output has a unique constant for each SEC/DIV setting between 100 and 100 ns. Each of these constants is set to 2048 when the instrument is cold started.

[°]For example, GN23 is the GN DAC output for side 3 of the CH 2 CCD; so side 3 is offset from sides 1, 2, and 4.

dEach CTxx DAC output has a unique constant for each SEC/DIV setting in both Normal and Envelope Acquire modes. Each of these constants is set to 2048 when the instrument is cold started.

^eFor example, CT14 is the CT DAC output for side 4 of the CH 1 CCD; so side 4 is offset from sides 1, 2, and 3.

Each CMxx DAC output constant varies with SEC/DIV setting: The first value given is for 50 ns; the second for 100 ns; and the third for 200 ns. SEC/DIV should be set accordingly when checking for correct voltage limits over DAC range.

Table 6-6 (cont)

	······································	Force DAC	Ranges				
DAC	DAC	· ·		Range	Effect of		
Output	Output Location	DAC Voltage After Cold Start	0	4095	Increasing Value		
CM20 U640-7		1650/0.27 V 2000/0.04 V	+4.76 +4.76	+12.1 +12.1	CH 2 CCD Sides 1 and 3 offset from 2 and 4.		
CM2E	U640-8	2200/—0.10 V 1650/—0.27 V 2000/—0.04 V 2200/—0.10 V	+4.76 +4.76 +4.76 +4.76	+12.1 +12.1 +12.1 +12.1	CH 2 CCD Sides 2 and 4 offset from 1 and 2.		
TRN19	U661-14 U631-14	200/1.24·V		=54 + 1:36 ::			
HORF	U631-8	100/1.30 V	1.37	+1.36			
JIT1 JIT2	U661-1 U661-7	1700/—2.54 V	-7.69	−2.23 V	Fast Ramp Slope increases for more counts per sec		
ALVL	U640-1	2176/0.09 V	−1.37 V	-1.36 V	Triggers at lower point		
GRAT	U520-10 U820-1	4095/14.66 V 4095/—3.34 V	0.83 V ^h 4.20 V	14.66 V -3.35 V	Decrease Grat intensity		
INTN NORM RDO1	U820-8 U820-7 U820-14	3160/0.78 V 1640/—0.28 V 2050/0 V	−1.37 V	1.36 V	Increases intensity		
CURS (CAL)	U610-3 U610-3 U610-4 U610-6	2048/—0.50	-1.37 V ~0 V ~0 V ~0 V	1.36 ~0 V ~0 V ~0 V	Current output into 75 Ω loads		
	U610-13 U610-15		~0 V ~0 V	0 V 0 V			
HORF	U631-8	100/-3.90 V	-4.11 V	4.09 V	Increases holdoff		
DACO DACG	U650-6 U660-6	2048/+0.04 V 3929/0.21 V	13.92 V 14.02 V	−13.15 V −13.32 V −5.18 V ⁱ	Unbalances DAC Uncalibrates DAC		

⁹Each TRNx DAC output has a unique constant for each VOLT/DIV setting between 2 mV and 50 mV. Each of these constants is set to 200 when the instrument is cold started.

hLimit at a DAC count of approximately 2000.

DACG (DAC Gain) interacts with DACO (DAC Offset); therefore, the DACG range can be limited if DACO is not centered. Changing either DACG or DACO causes the remaining DAC System outputs to be invalid until the correct settings for DAC Gain and Offset are rewritten into the DAC System.

HOLDOFF PROBLEMS

Trigger Holdoff Circuitry (schematic diagram 13):

Run Extended Diagnostic test 2600 for the SIDE-BOARD registers U761 and U762. If that falls, troubleshoot the indicated failure.

If not, troubleshoot the Trigger Holdoff circuitry.

1. Check the emitter voltages for logical HI/LO as follows:

SEC/DIV	Q761	Q771	Q772	Q783
500 ns	НІ	LO	LO	-15 V
1 <i>μ</i> s	LO	HI	LO	-15 V
10 μs	LO .	LO	HI	+5 V

If these levels are not correct, suspect the corresponding emitter diode, or the transistor emitter-base junctions as being defective. Observe that Q783 has no emitter diode, so suspect the transistor itself or Q782.

Some triggering failures are an indication of possible problems with the ATHO (A trigger holdoff signal). If ATHO is stuck HI, no triggers will be permitted by A/B Trigger Logic Array U150; if stuck LO, the triggering will be unstable.

Check the signals around flip-flop U872 for proper action of that device (see the test waveforms associated with the circuit next to schematic diagram 13).

Test scope: Select ENVELOPE 1 and AUTO TRIGGER MODE. Scope under test: Select 5 ns/div, trigger on the CAL signal, and set HOLDOFF to minimum.

SEQUENCER OUTPUT PROBLEMS

Sequencer Output circuitry (schematic diagram 20).

SEQUENCE OUT doesn't switch LO at the end of a sequence or back HI when the sequence is exited after completion:

- 1. Create a sequence with one step and no PAUSE. The front-panel setup is arbitrary for the step (see Operators Manual for operating the Sequencer).
- RECALL the sequence. Check that Q104's collector is HI before the sequence is recalled, switches LO at the end of a sequence, and switches back HI when the sequence is exited (see Operators Manual for operating the Sequencer).

If the collector switches properly, the problem is an open component in the R104-J125/P125-Flex Cable-J1903 path.

3. If collector doesn't switch, either the transistor, its collector supply, or its base drive is bad (CR104 may also be shorted). Isolate base drive to Q104 via R300 to determine whether drive or output circuitry is bad. The driving signal comes from I/O register block of schematic diagram 1.

SEQUENCER OUTPUT PROBLEMS

Sequencer Output circuitry (schematic diagram 20).

STEP OUT doesn't switch LO at the end of a sequence step or back HI at the start of the next sequence step:

1. Create a sequence containing at least two steps. The front panel setup is arbitrary for both steps, but set PAUSE on in the ACTIONS menu associated with the first step (see Operators Manual for operating the Sequencer).

2. Check that Q107's collector switches LO at the end of a step (should stay LO at end of PAUSE'd step 1) and back HI when the sequence is restarted (push PRGM).

If the collector switches properly, the problem is an open component in the R107-J125/P125-Flex Cable-J1904 path.

3. If collector doesn't switch, either the transistor, its collector supply, or its base drive is bad (CR107 may also be shorted). Isolate base drive to Q107 via R108 to determine whether the drive or output circuitry is bad.

The drive signal comes from I/O register block of schematic diagram 1.

5

GPIB CAPABILITY AVAILABLE FOR EXTENDED DIAGNOSTICS

Extended Diagnostics test may be run via the GPIB interface to track down failed devices when the Front Panel is locked up due to a front-panel failure or when there is no display visible. The importance of this is that the initial step of locating all problem areas is simplified when the 2440 can do it itself.

- 1. If the hardware and software are available to interface a 2440 to a GPIB controller, then run the Extended Diagnostics test. Troubleshoot any failed diagnostics test as indicated in Procedure 7.
- 2. If GPIB interface is not available, go to Procedure 6 to troubleshoot the display problem.

6

DISPLAY TROUBLESHOOTING

INTENSITY

No Intensity (HV Supply and CRT, schematic diagram 19):

If there is no GPIB capability, troubleshooting is going to be more difficult if no display is available. The steps in this table address the analog problems not detectable by the Extended Diagnostics in any case. Digital failures of the Display System are covered in the troubleshooting tables in the "Diagrams" section at the back of this manual.

- 1. Press STATUS to set READOUT level.
- 2. If no display is present, check the crt intensity grid voltage (V1000 pin 3), the grid bias adjust, the crt cathode and heater circuits, and the crt anode HV.

WARNING

A High Voltage probe is required to measure the grid, cathode, and anode voltage of the crt.

- 3. If no voltages are present, troubleshoot the HV power supply. The $-15\,\mathrm{V}$ Unreg supply is fused by F961 (schematic diagram 23) which will be open if a component failure in the HV power supply caused excessive loading.
- 4. If crt voltages are good, and still no intensity, turn off the 2440 and check the crt heater for continuity from pins 1 to 14. If open, change the crt.
- 5. Does intensity vary with the Grid Bias Adjust? If not, troubleshoot the DC Restorer circuit. If it does, check the signal from U227 at pin 13.
- Check input to U227 ZON on pin 3. If input ok, check supply voltages to U227. If all ok, change U227.

- If ZON not present, troubleshoot the Z-Axis Logic circuitry, U223C and input gates and signals (schematic diagram 17).
- If all ok in the crt and Z-Axis circuitry, go to the "No Display" troubleshooting tree at the back of this manual. Also, check that the Power-on Self Test completes without hanging. (See "System μP Halts in Power-up Test" following "No Intensity Control.")

No Intensity Control

- 1. Check signal output of U227 at pin 13. Is the waveform correct (see waveform 145 on schematic diagram 19), and does its amplitude vary with the DISP INTENSITY control? If yes, then check the signal path components to the junction of CR442 and R546 for continuity.
- If the signal at U227 pin 13 does not vary with the DISP INTENSITY control, check CR135 for open or short.
- 3. Check the ZINT signal on pin 2 of U227. Does it vary correctly with the DISP INTENSITY control?

 If yes, suspect U227. If no, then use the FORCE DAC test to verify the INTENSITY pot and the DAC SYSTEM.
- If the INTENSITY pot changes the DAC settings in the FORCE DAC test, the pot and potscanning circuitry are ok; if not, troubleshoot the Front Panel.
- 5. Check the suspected DAC outputs at the points indicated in the FORCE DAC test table. If DAC outputs are ok, troubleshoot Intensity multiplexer A10U811 (schematic diagram 6) and its select signals, and the Z-axis signal amplifiers (A10U810 and A10U812). Troubleshoot DAC circuit if the DAC outputs are bad (see the DAC System troubleshooting procedure).
- Check the DISDN signal at U414A pin 6 and the PRESTART + DISPLAY signal at U323A pin 3
 for correct operation (schematic diagram 17). If not correct, troubleshoot the Readout State
 Machine (see the "No Display" troubleshooting tree at the back of this manual).

SYSTEM µP HALTS IN POWER-UP TEST Test 3000—TRIG and READY LEDs on or Test 6000—READY and ARM LEDs on, and the 2440 Self Test has halted.

Problem is probably in the Display State Machine circuitry (schematic diagram 17) or the DISDN signal path to the System μP Interrupt circuit. Check that the DISDN signal is correct at U414 pin 6 (waveform 126 on schematic diagram 17); if not, troubleshoot the Display State Machine (see NO DISPLAY troubleshooting chart in the "Diagrams" section for typical Display State Machine waveforms). If the DISDN signal is ok, check the DISDN signal path to U580 pin 4 for continuity.

Test 8000-plus (+) LED on and Self Test has halted.

1. "Running Self Test" message is displayed, but nothing else is occurring.

Check the ACQDN signal at A11U670 (Time Base Controller).

2. No display is seen.

Check operation of the Readout State Machine.

FOCUS

If all the focus voltages and adjustments are correct in the following checks and proper focusing cannot be attained, suspect a defective crt. Check all the crt voltages and EXT CAL Display ADJUSTS for the crt to verify their accuracy before changing a suspected crt.

No Focus at Any Intensity:

- 1. Check the ASTIG adjustment.
- Check junction of R262 and R145 for a voltage swing of 0 to 15 V as the FOCUS pot is adjusted from one extreme to the other. If not correct, troubleshoot pot, connectors between the pot and the junction, and the 15 V supply to the FOCUS pot.
- 3. Check at the collector of Q152 for a voltage swing of $-175 \,\mathrm{V}$ to $-115 \,\mathrm{V}$ as the FOCUS pot is adjusted from one extreme to the other.
- Check for -300 V at the junction of R248 and R247. If not correct, check CR611, CR610, C618 and the 150 V peak ac supply.



An HV probe is required for the following step.

5. Check the intensity grid, cathode, and anode voltages for correct levels. If not correct, trouble-shoot faulty circuit.

Poor Focus at High Intensity:

- Check the HIGH DRIVE FOCUS adjustment.
- 2. Check the wiper of R400 for a varying voltage as the DISP INTENSITY is increased to high intensity levels. If not correct, check Q500, CR500 and VR316 for shorts or opens.
- 3. If the output of R400 tracks the display intensity changes, check R395, R297, C295, and P174.

Poor Edge Focus:

- 1. Check the EDGE FOCUS adjustment.
- 2. Check the collector of Q269 for a voltage swing of -131.8 V to -111.8 V as the EDGE FOCUS pot is adjusted from one extreme to the other. Check the wiper of R300 for a voltage swing of 0 to 50 V as the pot is adjusted from one extreme to the other. If not correct, check the pot and the +61 V supply.

DEFLECTION PROBLEM

Display Output (schematic diagram 18):

Vertical Deflection Bad (Horizontal stripe only) or Horizontal Deflection Bad (Vertical stripe only).

- 1. Press PRGM and then press the fifth menu selection button to do a PANEL INIT.
- Connect the CALIBRATOR output signal to the CH 1 BNC using one of the supplied 10X coded probes. Set the 2440 VOLTS/DIV setting to 200 mV. Press SAVE on the 2440, then MENU OFF.

- 3. Trigger the test scope on the ZON signal at U223 pin 8 (schematic diagram 17). Set the test scope Trigger Coupling to HF Reject and Slope to (minus).
- 4. Use the test scope to compare the circuit signals at the points indicated in schematic diagram 18 to the corresponding waveforms shown next to the diagram. (The HOLDOFF control will be of some use in obtaining a stable display if using an analog scope. If using a 2440 as the test scope, press SAVE to obtain a stable display, if necessary, for viewing.)
- 5. Troubleshoot as necessary if incorrect waveforms are found. If none of the waveforms are correct, problem is either U170 or bad input from the Vertical Display DAC, (U142) for bad vertical deflection. For bad horizontal deflection, problem is either U370B or bad input from the Horizontal Display DAC, U250. If bad input signals, troubleshoot the Display and Attributes Memory and Display DACs (schematic diagram 16). See "Distorted Display" troubleshooting chart at the back of this section.
- 6. If the waveform at U170 pin 6 is correct (or U370B pin 7 for the horizontal signal), but not correct at the integrator output, check that the sample switch (U270B) is getting the SAMPLE drive signal. Troubleshoot the Vertical or Horizontal vector generator circuitry.
- Is display switching correctly for dots, envelope, vector, and readout displays? If not, check multiplexer U290 and select signals (AMP0 and AMP1).

7

EXTENDED DIAGNOSTICS

If unfamiliar with the use or operation of the extended diagnostics routines of this scope, the calibration and diagnostics information supplied in the Diagnostics subsection of this section may prove very useful.

0000 EXTENDED DIAGNOSTICS

Running extended diagnostics at this level runs all tests. It is equivalent to SELF DIAG in the CAL/DIAG menu. A failed test is indicated by a FAIL label in the main Extended Diagnostics menu. Go to the lower testing levels of a failed test to isolate the failure.

1000 SYS-ROM

System ROM A12U670, A12U680, A12U682, A12U690, and A12U692 (schematic diagram 1)

Testing Method:

Run from this level, all ROM tests are selected in turn, or an individual test numbers 1100-1500 may be selected and run.

These tests compute the cyclic redundant word for the contents of the ROM. The resulting value is compared to the stored value of the first word of the ROM (the previously computed CRCC). A correct match indicates a good ROM.

If marked FAIL in the main Extended Diagnostic menu, go to the next level and run the test to determine the failed ROM or ROMs.

TEST NUMBER 1100: Test number 1100 tests U670, a 16K×8 ROM that contains the scope operating system. There are no sublevel tests for test number 1100.

TEST NUMBER 1200-1500: Test numbers 1200-1500 test the remaining four $64K\times8$ ROMs comprising the remainder of the System ROM memory, with numbers 1200, 1300, 1400, and 1500 testing U680 (ROM0.0), U682 (ROM0.1), U690 (ROM0.2), and U692 (ROM0.3), respectively. There are four sublevels to each test 1200-1500. This is because each ROM device is divided into four pages (16 Kbytes each) with each pages selectable by 2 address-page bits. Each sublevel test (1210-1240, 1310-1340, etc.) tests one of the four pages for a device.

For tests 1200-1500, the sublevel test number and the numerical suffix in the test label indicate the page and ROM device the test is run on. For instance, the sublevel test "1320 ROM0.1-5" is run on page 5 of 16 possible pages, where page 5 is part of ROM0.1 (U682).

The System Processor drives the System Address Decode circuitry to select the device and page from the System ROM. U890B provide the ROM0.0-3 chip select signals for selecting the ROM device accessed, and, if the ROM selected is one of the four paged ROMs, U860 supplies the page-selecting address bits, PAGE-BIT2 and PAGE-BIT3. Using test 1320 again as an example, U890B sets ROM0.0 LO to select ROM0.1 (U682), and U860 sets Page Bits 3 and 2 to LO (0) and HI (1), respectively, to select the second address page within the ROM device (the second page of that device is the 5th page of the 16 pages available for System ROM).

NOTE

The page number associated with the sublevel test labels are based on viewing the 16-page memory as having the following sequence: the first four pages (pages 0-3) are located in the first four 16-Kbyte address spaces of ROM0.0-ROM0.3, respectively; the second four pages (4-7) in the second four 16-Kbyte address spaces, respectively; etc. That is why, in the previous example, the label for test level 1320 is "ROM0.1-5" where "-5" indicates the fifth page. Page 5 is the fifth page for the entire paged-System ROM; it is the second page (or 16-kbyte memory space) for U682.

Troubleshooting Procedure:

1. A failed ROM test indicates a defective ROM. Check that the correct ROMs are installed in the correct sockets.

Check out the supply voltages and the chip select to a failed ROM to verify them.

2. A failure of most or all paged ROM indicates a paging chip select problem. The last condition is probably not detectable as the System μP is unable to obtain it operating instructions from the ROM. The System μP Kernel test (given in Procedure 8) may be used to check that the microprocessor is operating and to check the chip-select addressing circuitry for correct operation.

1100 ROM1	Base page ROM, A12U670		 	
1210 ROM0.0-	1st quarter of A12U680 (page 0)	 -		
1220 ROM0.0-4	2nd quarter of A12U680 (page 4)			
1230 ROM0.0-8	3rd quarter of A12U680 (page 8)			
1240-ROM0.0-C	4th-quarter-of-A12U680 (-page C-)			
1310 ROM0.1-1	1st quarter of A12U682 (page 1)			1.4
1310 ROM0.1-5	2nd quarter of A12U682 (page 5)			

Table 6-6 (cont)

numbers 2100 through 2600. If marked FAIL in the main Extended Diagnostics menu, move the curse to the 2000 level test and rerun to find next lower failure level in the Registers tests. All register names have the convention of assuming the name given to the schematic-designated chip select line for that register (i.e., MISC is the name of the chip select on the time base/display board to registers U532 and U540). The register tests are organized by circuit board. Where possible, a set of four bit patterns have bee used. The register tests have the capability of testing for stuck bits (both high and low) for each data line as well as testing each data line for interconnecting shorts to other data lines. If all bit patterns of a test fail, check for a defective chip select, a defective IC in the chip-select patt or possibly the part under test is defective. If at least one bit pattern passes, use the "which be changed" method of isolating which bit(s) have the problem. System μP Register Tests—A12 Circuit Board: Testing Method: The processor board has nine register tests. These are organized from the System μP outward for		
1310 ROM0.1-D 4th quarter of A12U692 (page D) 1410 ROM0.2-6 2nd quarter of A12U690 (page 2) 1410 ROM0.2-6 2nd quarter of A12U690 (page 6) 1410 ROM0.2-E 3rd quarter of A12U690 (page B) 1410 ROM0.2-E 4th quarter of A12U690 (page B) 1510 ROM0.3-B 1st quarter of A12U692 (page B) 1510 ROM0.3-7 2nd quarter of A12U692 (page B) 1510 ROM0.3-B 3rd quarter of A12U692 (page B) 1510 ROM0.3-F 4th quarter of A12U692 (page B) 1510 ROM0.3-F 4th quarter of A12U692 (page B) 1510 ROM0.3-F 3rd quarter of A12U692 (page B) 1510 ROM0.3-F 4th quarter of A12U692 (page B) 1510 ROM0.3-F 3rd quarter of A12U692 (page B) 1510 ROM0.3-F 4th quarter of A12U692 (page B) 1510 ROM0.3-F 4th quarter of A12U692 (page B) 1510 ROM0.3-F 3rd quarter of A12U692 (page B) 1510 ROM0.3-F 4th quarter of A12U692 (page B) 1510 ROM0.3-F 4th quarter of A12U692 (page B) 1510 ROM0.3-F 4th quarter of A12U692 (page B) 1510 ROM0.3-F 4th quarter of A12U692 (page B) 1510 ROM0.3-F 4th quarter of A12U692 (page B) 1510 ROM0.3-F 5rd quarter of A12U692 (page B) 1510 ROM0.3-F 5rd quarter of A12U692 (page B) 1510 ROM0.3-F 5rd quarter of A12U692 (page B) 1510 ROM0.3-F 5rd quarter of A12U692 (page B) 1510 ROM0.3-F 5rd quarter of A12U692 (page B) 1510 ROM0.3-F 7 8rd quarter of A12U692 (page B) 1510 ROM0.3-F 7 8rd quarter of A12U692 (page B) 1510 ROM0.3-F 7 8rd quarter of A12U692 (page B) 1510 ROM0.3-F 7 8rd quarter of A12U692 (page B) 1510 ROM0.3-F 7 8rd quarter of A12U692 (page B) 1510 ROM0.3-F 7 8rd quarter of A12U692 (page B) 1510 ROM0.3-F 7 8rd quarter of A12U692 (page B) 1510 ROM0.3-F 7 8rd quarter of A12U692 (page B) 1510 ROM0.3-F 7 8rd quarter of A12U692 (page B) 1510 ROM0.3-F 7 8rd quarter of A12U692 (page B) 1510 ROM0.3-F 7 8rd quarter of A12U692 (page B) 1510 ROM0.3-F 7 8rd quarter of A12U692 (page B) 1510 ROM0.3-F 7 8rd quarter of A12U692 (page B) 1510 ROM0.3-F 7 8rd quarter of A12U692 (page B) 1510 ROM0.3-F 7 8rd quarter of A12U692 (page B) 1510 R	1310 ROM0.1-9	
1410 ROM0.2-6 2nd quarter of A12U690 (page 6) 1410 ROM0.2-A 3rd quarter of A12U690 (page E) 1510 ROM0.3-B 3rd quarter of A12U692 (page 3) 1510 ROM0.3-7 2nd quarter of A12U692 (page 7) 1510 ROM0.3-B 3rd quarter of A12U692 (page B) * Not used 1510 ROM0.3-F 4th quarter of A12U692 (page B) * Not used 1510 ROM0.3-F 4th quarter of A12U692 (page F) * Not used 2000 Registers Testing: Testing Method: From this level, all register tasts are selected in turn. Individual tests may be executed by selecting te numbers 2100 through 2800. If marked FAIL in the main Extended Diagnostics menu, move the curse to the 2000 level test and rerun to find next tower failure level in the Registers tests. All register names have the convention of assuming the name given to the schematic-designated chip select line for that register (i.e., MISC is the name of the chip select on the time base/display board in registers tests are organized by circuit board. Where possible, a set of four bit patterns have bee used. The register tests have the capability of testing for stuck bits (both high and low) for each dat line as well as testing each data line for interconnecting shorts to other data lines. If all bit patterns of a test fail, check for a defective chip select, a defective IC in the chip-select patt or possibly the part under test is defective. If at least one bit pattern passes, use the "which behanged" method of isolating which bit(s) have the problem. 2100 System \(\mu \) Register Tests—A12 Circuit Board: Testing Method: The processor board has nine register tests. These are organized from the System \(\mu \) Doubton, investication investication.	1310 ROM0.1-D	
1410 ROM0.2-A 3rd quarter of A12U690 (page A) 1410 ROM0.2-E 4th quarter of A12U690 (page E) 1510 ROM0.3-3 1st quarter of A12U692 (page 3) 1510 ROM0.3-7 2nd quarter of A12U692 (page 7) 1510 ROM0.3-B 3rd quarter of A12U692 (page B) * Not used 1510 ROM0.3-F 4th quarter of A12U692 (page F) * Not used 2000 Registers Testing: Testing Method: From this level, all register tests are selected in turn. Individual tests may be executed by selecting te numbers 2100 through 2600. If marked FAIL in the main Extended Diagnostics menu, move the curse to the 2000 level test and rerun to find next lower failure level in the Registers tests. All register names have the convention of assuming the name given to the schematic-designated chis select line for that register (i.e., MISC is the name of the chip select on the time base/display board in registers US52 and US40). The register tests are organized by circuit board. Where possible, a set of four bit patterns have bee used. The register tests have the capability of testing for stuck bits (both high and low) for each dat line as well as testing each data line for interconnecting shorts to other data lines. If all bit patterns of a test fall, check for a defective chip select, a defective IC in the chip-select patt or possibly the part under test is defective. If at least one bit pattern passes, use the "which be changed" method of isolating which bit(s) have the problem. 2100 System µF Register Tests—A12 Circuit Board: Testing Method: The processor board has nine register tests. These are organized from the System µP outward for increasing confidence. One should always check multiple failures from top to bottom, investigation.	1410 ROM0.2-2	1st quarter of A12U690 (page 2)
1510 ROM0.3-3 1st quarter of A12U692 (page 3) 1510 ROM0.3-7 2nd quarter of A12U692 (page 7) 1510 ROM0.3-B 3rd quarter of A12U692 (page B) * Not used 2000 Registers Testing: Testing Method: From this level, all register tests are selected in turn, individual tests may be executed by selecting te numbers 2100 through 2600. If marked FAIL in the main Extended Diagnostics menu, move the curse to the 2000 level test and errun to find next lower failure level in the Registers tests. All register names have the convention of assuming the name given to the schematic-designated chipselect line for that register (i.e., MISC is the name of the chip select on the time base/display board registers US32 and U540). The register tests are organized by circuit board. Where possible, a set of four bit patterns have bee used. The register tests have the capability of testing for stuck bits (both high and low) for each dat line as well as testing each data line for interconnecting shorts to other data lines. If all bit patterns of a test fail, check for a defective chip select, a defective IC in the chip-select pattor possibly the part under, test is defective. If at least one bit pattern passes, use the "which be changed" method of isolating which bit(s) have the problem. 2100 System μP Register Tests—A12 Circuit Board: Testing Method: The processor board has nine register tests. These are organized from the System μP outward for increasing confidence. One should always check multiple failures from top to bottom, investicating increasing confidence. One should always check multiple failures from top to bottom, investicating testing the chip and the chip-select pattern passes in the processor pound has nine register tests. These are organized from the System μP outward for increasing confidence. One should always check multiple failures from top to bottom, investicating the chip and the chip-select pattern passes.	1410 ROM0.2-6	2nd quarter of A12U690 (page 6)
1510 ROM0.3-3 1st quarter of A12U692 (page 7) 2nd quarter of A12U692 (page 7) 3rd quarter of A12U692 (page 8) * Not used 3rd quarter of A12U692 (page F) * Not used 4th quarter of A12U692 (page F) * Not used Registers Testing: Testing Method: From this level, all register tests are selected in turn. Individual tests may be executed by selecting te numbers 2100 through 2600. If marked FAIL in the main Extended Diagnostics menu, move the curse to the 2000 level test and rerun to find next lower failure level in the Registers tests. All register names have the convention of assuming the name given to the schematic-designated chip select line for that register (i.e., MISC is the name of the chip select on the time base/display board is registers U532 and U540). The register tests are organized by circuit board. Where possible, a set of four bit patterns have bee used. The register lests have the capability of testing for stuck bits (both high and low) for each dat line as well as testing each data line for interconnecting shorts to other data lines. If all bit patterns of a test fail, check for a defective chip select, a defective IC in the chip-select patt or possibly the part under test is defective. If at least one bit pattern passes, use the "which be changed" method of isolating which bit(s) have the problem. System μP Register Tests—A12 Circuit Board: Testing Method: The processor board has nine register tests. These are organized from the System μP outward for increasing confidence. One should always check multiple failures from top to bottom, investicating the content of the chip selection increasing confidence. One should always check multiple failures from top to bottom, investicating the content of the chip selection increasing confidence.	1410 ROM0.2-A	3rd quarter of A12U690 (page A)
2nd quarter of A12U692 (page F)* Not used 3rd quarter of A12U692 (page B) * Not used 4th quarter of A12U692 (page F) * Not used Registers Testing: Testing Method: From this level, all register tests are selected in turn: Individual tests may be executed by selecting te numbers 2100 through 2600. If marked FAIL in the main Extended Diagnostics menu, move the curse to the 2000 level test and rerun to find next lower failure level in the Registers tests. All register names have the convention of assuming the name given to the schematic-designated chip select line for that register (i.e., MISC is the name of the chip select on the time base/display board registers U532 and U540). The register tests are organized by circuit board. Where possible, a set of four bit patterns have bee used. The register tests have the capability of testing for stuck bits (both high and low) for each dat line as well as testing each data line for interconnecting shorts to other data lines. If all bit patterns of a test fail, check for a defective chip select, a defective IC in the chip-select patt or possibly the part under test is defective. If at least one bit pattern passes, use the "which be changed" method of isolating which bit(s) have the problem. System µP Register Tests—A12 Circuit Board: Testing Method: The processor board has nine register tests. These are organized from the System µP outward for increasing confidence. One should always check multiple failures from top to bottom, investicating	1410 ROM0.2-E	4th quarter of A12U690 (page E)
3rd quarter of A12U692 (page B) * Not used 4th quarter of A12U692 (page F) * Not used Registers Testing: Testing Method: From this level, all register tests are selected in turn: Individual tests may be executed by selecting te numbers 2100 through 2600. If marked FAIL in the main Extended Diagnostics menu, move the curse to the 2000 level test and rerun to find next lower failure level in the Registers tests. All register names have the convention of assuming the name given to the schematic-designated chip select line for that register (i.e., MISC is the name of the chip select on the time base/display board registers U532 and U540). The register tests are organized by circuit board. Where possible, a set of four bit patterns have bee used. The register tests have the capability of testing for stuck bits (both high and low) for each dat line as well as testing each data line for interconnecting shorts to other data lines. If all bit patterns of a test fail, check for a defective chip select, a defective IC in the chip-select patt or possibly the part under test is defective. If at least one bit pattern passes, use the "which be changed" method of isolating which bit(s) have the problem. System μP Register Tests—A12 Circuit Board: Testing Method: The processor board has nine register tests. These are organized from the System μP outward for increasing confidence. One should always check multiple failures from top to bottom, investicating the confidence of the chips and the confidence of the should always check multiple failures from top to bottom, investicating the confidence of the chips and the chips and the confidence of the chips and	1510 ROM0.3-3	1st quarter of A12U692 (page 3)
1510 ROM0.3-F 4th quarter of A12U692 (page F) * Not used Registers Testing: Testing Method: From this level, all register tests are selected in turn: Individual tests may be executed by selecting te numbers 2100 through 2600. If marked FAIL in the main Extended Diagnostics menu, move the curse to the 2000 level test and rerun to find next lower failure level in the Registers tests. All register names have the convention of assuming the name given to the schematic-designated chip select line for that register (i.e., MISC is the name of the chip select on the time base/display board registers U532 and U540). The register tests are organized by circuit board. Where possible, a set of four bit patterns have bee used. The register tests have the capability of testing for stuck bits (both high and low) for each dat line as well as testing each data line for interconnecting shorts to other data lines. If all bit patterns of a test fail, check for a defective chip select, a defective IC in the chip-select patt or possibly the part under test is defective. If at least one bit pattern passes, use the "which be changed" method of isolating which bit(s) have the problem. System μP Register Tests—A12 Circuit Board: Testing Method: The processor board has nine register tests. These are organized from the System μP outward for increasing confidence. One should always check multiple failures from top to bottom, investigating the part of the contraction of the should always check multiple failures from top to bottom, investigating the part of the contraction of the should always check multiple failures from top to bottom, investigating the part of the contraction of the should always check multiple failures from top to bottom, investigating the part of the contraction of t	1510 ROM0.3-7	2nd quarter of A12U692 (page 7)
REG Registers Testing: Testing Method: From this level, all register tests are selected in turn. Individual tests may be executed by selecting te numbers 2100 through 2600. If marked FAIL in the main Extended Diagnostics menu, move the curso to the 2000 level test and rerun to find next lower failure level in the Registers tests. All register names have the convention of assuming the name given to the schematic-designated chip select line for that register (i.e., MISC is the name of the chip select on the time base/display board to registers U532 and U540). The register tests are organized by circuit board. Where possible, a set of four bit patterns have bee used. The register tests have the capability of testing for stuck bits (both high and low) for each data line as well as testing each data line for interconnecting shorts to other data lines. If all bit patterns of a test fail, check for a defective chip select, a defective IC in the chip-select patt or possibly the part under test is defective. If at least one bit pattern passes, use the "which be changed" method of isolating which bit(s) have the problem. System μP Register Tests—A12 Circuit Board: Testing Method: The processor board has nine register tests. These are organized from the System μP outward for increasing confidence. One should always check multiple failures from top to bottom, investigating the content of the con	1510 ROM0.3-B	3rd quarter of A12U692 (page B) * Not used
Testing Method: From this level, all register tests are selected in turn. Individual tests may be executed by selecting te numbers 2100 through 2600. If marked FAIL in the main Extended Diagnostics menu, move the curse to the 2000 level test and rerun to find next lower failure level in the Registers tests. All register names have the convention of assuming the name given to the schematic-designated chip select line for that register (i.e., MISC is the name of the chip select on the time base/display board to registers U532 and U540). The register tests are organized by circuit board. Where possible, a set of four bit patterns have been used. The register tests have the capability of testing for stuck bits (both high and low) for each data line as well as testing each data line for interconnecting shorts to other data lines. If all bit patterns of a test fail, check for a defective chip select, a defective IC in the chip-select patt or possibly the part under test is defective. If at least one bit pattern passes, use the "which be changed" method of isolating which bit(s) have the problem. System \(\mu \) Register Tests—A12 Circuit Board: Testing Method: The processor board has nine register tests. These are organized from the System \(\mu \) Poutward for increasing confidence. One should always check multiple failures from top to bottom, investigating	1510 ROM0.3-F	4th quarter of A12U692 (page F) * Not used
From this level, all register tests are selected in turn. Individual tests may be executed by selecting te numbers 2100 through 2600. If marked FAIL in the main Extended Diagnostics menu, move the curso to the 2000 level test and rerun to find next lower failure level in the Registers tests. All register names have the convention of assuming the name given to the schematic-designated chip select line for that register (i.e., MISC is the name of the chip select on the time base/display board to registers U532 and U540). The register tests are organized by circuit board. Where possible, a set of four bit patterns have bee used. The register tests have the capability of testing for stuck bits (both high and low) for each data line as well as testing each data line for interconnecting shorts to other data lines. If all bit patterns of a test fail, check for a defective chip select, a defective IC in the chip-select patt or possibly the part under test is defective. If at least one bit pattern passes, use the "which be changed" method of isolating which bit(s) have the problem. 2100 System μP Register Tests—A12 Circuit Board: Testing Method: The processor board has nine register tests. These are organized from the System μP outward for increasing confidence. One should always check multiple failures from top to bottom, investigating		Registers Testing:
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increasing confidence. One should always check multiple failures from top to bottom, investigating		Testing Method:
		The processor board has nine register tests. These are organized from the System μP outward for increasing confidence. One should always check multiple failures from top to bottom, investigating each in turn.